Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC Wrapper v1.8

DS550 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-5 FPGA Embedded Tri-Mode Ethernet MAC Wrapper automates the generation of HDL wrapper files for the Embedded Tri-Mode Ethernet MAC (Ethernet MAC) in Virtex-5 LXT, SXT, FXT and TXT FPGAs using the Xilinx® CORE Generator™ software.

VHDL and Verilog instantiation templates are available in the Libraries Guide for the Virtex-5 FPGA Ethernet MAC primitive; however, due to the complexity and large number of ports, the CORE Generator software simplifies integration of the Ethernet MAC by providing HDL examples based on user-selectable configurations.

Features

- Allows selection of one or both Ethernet MACs (EMAC0/EMAC1) from the Ethernet MAC primitive
- Sets the EMAC0/EMAC1 attributes based on user options
- Provides user-configurable Ethernet MAC physical interfaces
  - Supports MII, GMII, RGMII v1.3, RGMII v2.0, SGMII, and 1000BASE-X PCS/PMA interfaces
  - Instantiates clock buffers, DCMs, Virtex-5 FPGA RocketIO™ GTP or GTX transceivers, and logic as required for the selected physical interfaces
- Provides a simple FIFO-loopback example design, connected to the MAC client interfaces
- Provides a simple demonstration test bench based on the selected configuration
- Generates VHDL or Verilog

LogiCORE IP Facts Table					
Supported Device Family[1]	Virtex-5				
Supported User Interfaces	LocalLink (when using provided example FIFO), Client I/F				
Performance	10 Mb/s, 100 Mb/s, 1 Gb/s				
Resources[2]					
	LUTs	**FFs**	**Block RAMs**	**DCM**	**BUFG**
	380-930	440-1220	(18k) 4-10	0-1	2-10
Provided with Wrapper					
Documentation	Product Specification Getting Started Guide User Guide[3]				
Design Files	VHDL and/or Verilog				
Example Designs	Example FIFO connected to Client I/F				
Test Bench	Demonstration Test Bench, Scripts				
Constraints File	User Constraints File (.ucf)				
Simulation Model	Verilog SecureIP model [4]				
Tested Design Tools					
Design Entry Tools	ISE 13.1 software				
Simulation Tools	Mentor Graphics ModelSim v6.6d [4] Cadence Incisive Enterprise Simulator (IES) v10.2 [4] Synopsys VCS and VCS MX 2010.06 [4]				
Synthesis	XST 13.1				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.
2. The precise number depends on user configuration; see Device Utilization.
3. Available from www.xilinx.com/support/documentation/ip_documentation/ug194.pdf.
4. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Ethernet Architecture Overview

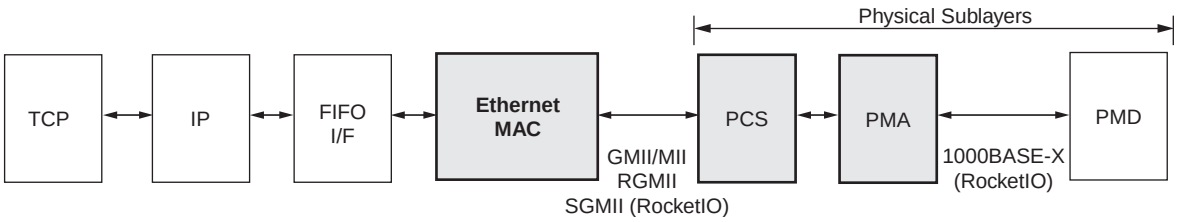

Figure 1: **Typical Ethernet Architecture**

Figure 1 displays the Ethernet MAC architecture from the MAC to the right, as defined in the *IEEE 802.3* specification, and also illustrates where the supported physical interfaces fit into the architecture.

MAC

The Ethernet MAC is defined in the *IEEE 802.3* specification clauses 2, 3, and 4. A MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can connect to, any type of physical sublayer.

GMII/MII

The Media Independent Interface (MII), defined in *IEEE 802.3* clause 22, is a parallel interface that connects a 10-Mb/s and/or 100-Mb/s capable MAC to the physical sublayers. The Gigabit Media Independent Interface (GMII), defined in *IEEE 802.3* clause 35, is an extension of the MII used to connect a 1-Gb/s capable MAC to the physical sublayers. MII can be considered a subset of GMII, and as a result, GMII/MII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s.

RGMII

The Reduced-GMII (RGMII) is an alternative to GMII/MII. RGMII achieves a 50-percent reduction in the pin count, achieved by the use of double-data-rate (DDR) flip-flops. For this reason, RGMII is preferred over GMII by PCB designers. RGMII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s.

SGMII

The Serial-GMII (SGMII) interface is an alternative to GMII/MII. SGMII converts the parallel interface of the GMII/MII into a serial format using a RocketIO GTP or GTX transceiver, radically reducing the I/O count. For this reason, it is often the preferred interface of PCB designers. SGMII can carry Ethernet traffic at 10 Mb/s, 100 Mb/s, and 1 Gb/s.

PCS, PMA, PMD

The combination of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) sublayer comprise the physical layers of the Ethernet protocol.

Two main physical standards are specified for Ethernet:

- BASE-T, a copper standard using twisted pair cabling systems
- BASE-X, usually a fibre optical physical standard using short and long wavelength laser

BASE-T devices, supporting 10 Mb/s, 100 Mb/s, and 1 Gb/s Ethernet speeds, are readily available as off-the-shelf parts. As illustrated in Figure 1 and Figure 2, these can be connected using GMII/MII, RGMII, or SGMII to provide a tri-speed Ethernet port.

The Ethernet MAC has built-in 1000BASE-X PCS/PMA functionality and can be connected to a RocketIO GTP or GTX transceiver to provide a 1 Gb/s fibre optic port, as illustrated in Figure 3.

Applications

Typical applications for the Ethernet MAC core include

- Ethernet Tri-Speed BASE-T Port
- Ethernet 1000BASE-X Port

Ethernet Tri-Speed BASE-T Port

Figure 2 illustrates a typical application for a single Ethernet MAC. The PHY side of the core is implementing an external GMII/MII by connecting it to IOBs; the external GMII/MII is connected to an off-the-shelf Ethernet PHY device, which performs the BASE-T standard at 1 Gb/s, 100 Mb/s, and 10 Mb/s speeds. Alternatively, the external GMII/MII can be replaced with an RGMII (as shown) or as an SGMII (which requires the use of a RocketIO GTP or GTX transceiver). GMII, RGMII, and SGMII functionality are demonstrated in the HDL examples provided with the example design.

The client side of the Ethernet MAC is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO (delivered with the example design) to complete a single Ethernet port. This port is displayed connected to a Switch or Routing matrix, which can contain several ports.

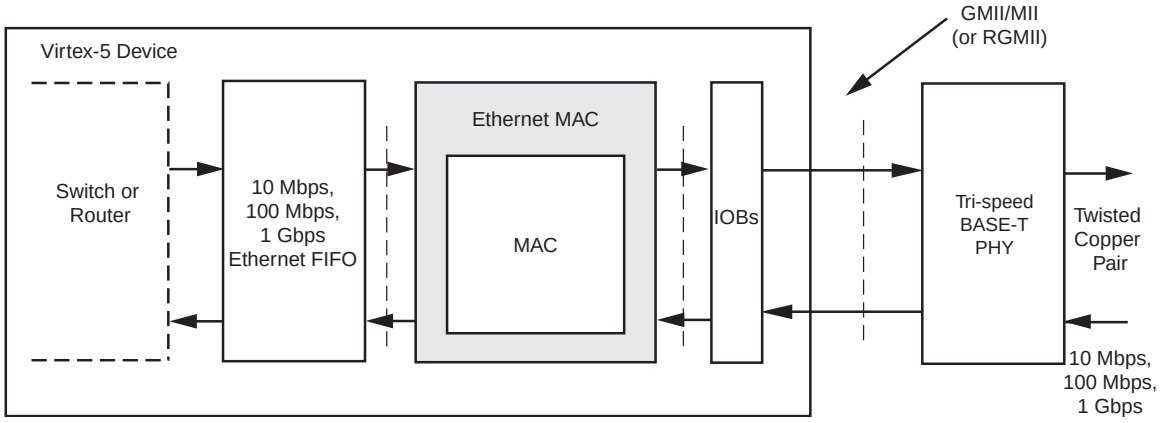

Figure 2: **Typical 1000BASE-T Application**

Ethernet 1000BASE-X Port

Figure 3 illustrates a typical application for a single Ethernet MAC. The PHY side of the MAC is connected to a RocketIO GTP or GTX transceiver, which in turn is connected to an external off-the-shelf GBIC or SFP optical transceiver. The 1000BASE-X logic can be optionally provided by the Ethernet MAC, as displayed. 1000BASE-X functionality is demonstrated in the HDL examples provided with the example design.

The client side of the Ethernet MAC is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO (delivered with the example design) to complete a single Gigabit Ethernet port. This port is connected to a Switch or Router matrix, which can contain several ports.

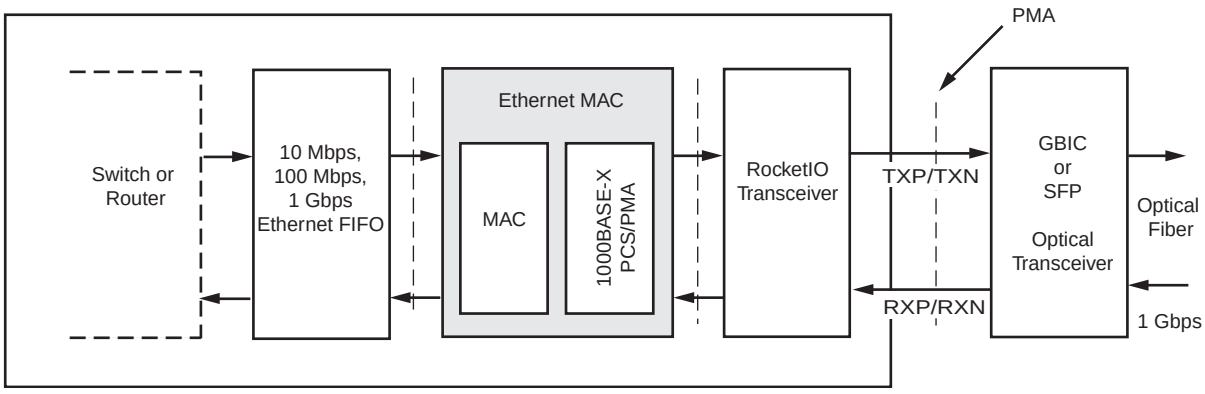

Figure 3: **Typical 1000BASE-X Application**

Example Design Overview

Figure 4 illustrates the major functional blocks of the Ethernet MAC example design. All illustrated components are provided in HDL, with the exception of the Ethernet MAC component.

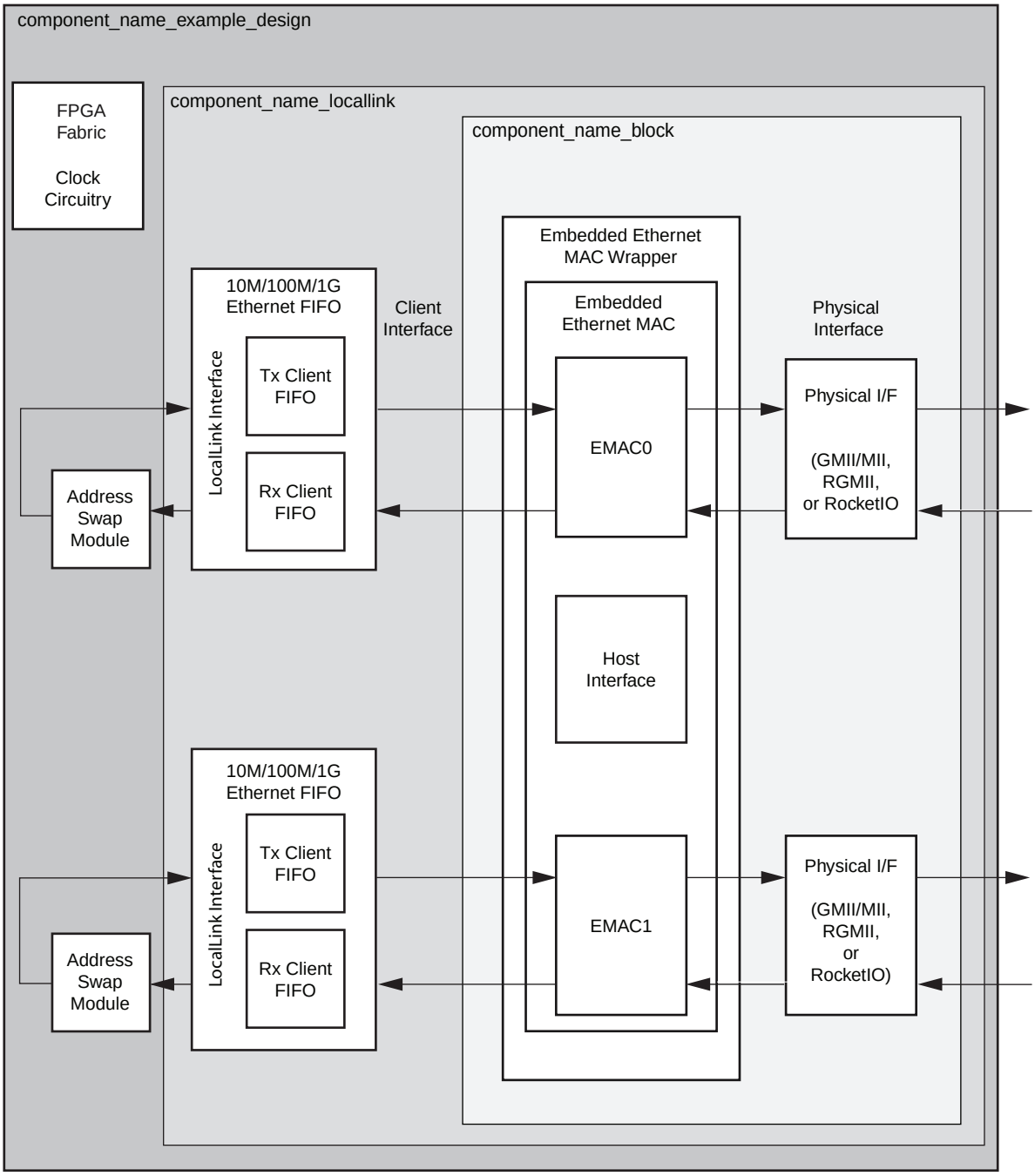

Figure 4: **Example Design**

Ethernet MAC Example Design

The example design is arranged for quick adaptation and can be downloaded onto an FPGA to provide a real hardware test environment. In addition, all the clock management logic required to operate the Ethernet MAC and its example design is provided. DCMs, BUFGs, and so forth are instantiated as required.

The data is looped back at the client interface, enabling the Ethernet MAC to be quickly connected to a protocol tester—frames injected into the Ethernet MAC PHY Receive port are relayed back through the Ethernet MAC and out through the Ethernet MACs PHY Transmit port. Using this method, they are received back at the protocol tester.

The design includes an Address Swapping Module and a FIFO. Frames received by the Ethernet MAC are passed through the Receive side of the FIFO. Data from the Receive side of the FIFO is passed into the Address Swap Module and then on to the Transmit side of the FIFO using a LocalLink interface. The Transmit FIFO queues frames for transmission and connects directly to the client side Transmit interface of the Ethernet MAC.

Address Swap Module

The Address Swap Module switches the Destination Address and Source Address within the received MAC frame. Using this method, frames received from a link partner, for example a protocol tester, are relayed back to the correct Destination Address.

10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO

The 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO is a wrapper file around the Receive and Transmit FIFO components. These components can be used in more complex client applications, as illustrated in Figure 2 and Figure 3. To use the FIFOs, the component_name_locallink component can be instantiated in the user design.

Receive Client FIFO

The Receive (Rx) Client FIFO, a 4k-byte FIFO implemented in block RAMs, can be used for more complex client applications and can be connected directly to the Rx Client Interface of the Ethernet MAC. The Rx Client provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO drops all frames marked as bad from the Ethernet MAC so that only error-free frames are passed to the Ethernet client.

Transmit Client FIFO

The Transmit (Tx) Client FIFO, a 4k-byte FIFO implemented in block RAMs, can used for more complex client applications and can be connected directly to the Tx Client Interface of the Ethernet MAC. The Tx Client FIFO provides a LocalLink connection for the user.

- The FIFO operates at all Ethernet speeds supported by the Ethernet MAC.
- The FIFO is capable of half-duplex re-transmission. For this reason, if a collision occurs on the medium, the Ethernet MAC indicates a collision on the Tx Client interface and the FIFO automatically re-queues the frame for re-transmission.

Ethernet MAC Wrapper

The Ethernet MAC wrapper file instantiates the full Ethernet MAC primitive. For one or both Ethernet MACs (EMAC0/EMAC1), the following applies:

- All unused input ports on the primitive are tied to the appropriate logic level; all unused output ports are left unconnected.
- The Ethernet MAC attributes are set based on options selected in the CORE Generator software.
- Only used ports are connected to the ports of the wrapper file.

This simplified wrapper should be used as the instantiation template for the Ethernet MAC in customer designs.

Physical I/F

An appropriate Physical Interface is provided for each selected EMAC0/EMAC1. This interface connects the physical interface of the Ethernet MAC block to the I/O of the FPGA. As required, the following components are provided:

- For GMII/MII, this component contains Input/Output block (IOB) buffers and IOB flip-flops.
- For RGMII, this component contains contain IOB buffers, IOB Double-Data Rate flip-flops and IODELAY elements to align the incoming data with the receiver clock. An IODELAY element is also used to delay the transmitted clock in RGMII V2.0.
- For 1000BASE-X PCS/PMA or SGMII, this component instantiates and connects a RocketIO GTP or GTX transceiver.

Device Utilization

The following sections provide approximate device-utilization figures for common configurations of the Ethernet MAC and its example design:

- 1 Gb/s Only Operation
- Tri-Speed Operation
- 100 Mb/s or 10 Mb/s Operation

Of interest is the utilization of clock resources, specifically the global clock usage (BUFGs), which should influence the selection of the interface type. These clock resource figures do not consider any clock that can be used for the Host Interface.

1 Gb/s Only Operation

Table 1 defines approximate utilization figures for common configurations of the Ethernet MAC and its example design for 1 Gb/s operation.

Table 1: **Device Utilization for 1 Gb/s Operation**

Parameter Values		Device Resources				
Physical Interface	**Ethernet MAC Usage**	**LUTs**	**Registers**	**18K Block RAMs**	**BUFGs**	**DCMs**
GMII	Single EMAC	380	450	4	2[1]	0
	Both EMACs	760	880	8	3[1]	0
RGMII 1.3	Single EMAC	380	460	4	2[1]	0
	Both EMACs	760	900	8	3[1]	0
RGMII 2.0	Single EMAC	380	460	4	2[1]	0
	Both EMACs	760	900	8	3[1]	0
SGMII	Single EMAC	390	440	4	1	0
	Both EMACs	780	870	8	1	0
1000BASE-X (8-bit client)	Single EMAC	390	440	4	1	0
	Both EMACs	780	870	8	1	0
1000BASE-X (16-bit client)	Single EMAC	370	560	4	3	1
	Both EMACs	730	1120	8	3	1

1. These implementations use IDLEAY elements, which require a 200 MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.

Tri-Speed Operation

Table 2 defines approximate utilization figures for common configurations of the Ethernet MAC and its example design 10 Mb/s, 100 Mb/s, or 1 Gb/s operation.

Table 2: **Device Utilization for Tri-Speed Operation**

Parameter Values		Device Resources				
Physical Interface	**Ethernet MAC Usage**	**LUTs**	**Registers**	**18K Block RAMs**	**BUFGs**	**RCLKs**
GMII/MII (standard clocking)	Single EMAC	400	480	4	5[1]	0
	Both EMACs	790	950	8	10[1]	0
GMII/MII (with clock enable)	Single EMAC	400	500	4	2[1]	0
	Both EMACs	790	980	8	4[1]	0
GMII/MII (with byte PHY)	Single EMAC	410	510	4	2[1]	0
	Both EMACs	810	990	8	4[1]	0
RGMII 1.3 (standard clocking)	Single EMAC	400	490	4	4[1]	0
	Both EMACs	790	970	8	8[1]	0
RGMII 1.3 (with clock enable)	Single EMAC	400	510	4	2[1]	0
	Both EMACs	790	1000	8	4[1]	0
RGMII 2.0 (standard clocking)	Single EMAC	400	490	4	4[1]	0
	Both EMACs	790	970	8	8[1]	0
RGMII 2.0 (with clock enable)	Single EMAC	400	510	4	2[1]	0
	Both EMACs	790	1000	8	4[1]	0
SGMII	Single EMAC	470	620	5	2	1
	Both EMACs	930	1220	10	3	2

1. These implementations use IDLEAY elements, which require a 200 MHz reference clock for the associated IDELAYCTRL. The reference clock's BUFG is not accounted for.

100 Mb/s or 10 Mb/s Operation

Table 3 provides approximate utilization figures for common configurations of the Ethernet MAC and its example design for 10 Mb/s or 100 Mb/s operation. For all other interfaces, see Tri-Speed Operation.

Table 3: **Device Utilization for 10 Mb/s, 100 Mb/s Operation**

Parameter Values		Device Resources			
Physical Interface	**Ethernet MAC Usage**	**LUTs**	**Registers**	**18K Block RAMs**	**BUFGs**
MII (standard clocking)	Single EMAC	400	460	4	4
	Both EMACs	780	920	8	8
MII (with clock enable)	Single EMAC	390	480	4	2
	Both EMACs	780	950	8	4
MII (with byte PHY)	Single EMAC	400	480	4	2
	Both EMACs	800	960	8	4

Ordering Information

The Ethernet MAC wrapper is provided under the End User License Agreement and can be generated using CORE Generator software v13.1 and higher. The CORE Generator software is shipped with Xilinx ISE® Design Suite Series Development software.

In ISE v12.1 software and later, a license key is not required to access the IP. To access the wrapper in ISE v11.4 software and older, a no cost full license must be obtained from Xilinx. See the product page:

www.xilinx.com/products/ipcenter/V5_Embedded_TEMAC_Wrapper.htm

Contact your local Xilinx sales representative for pricing and availability of other Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Spelled Out
DCM	Digital Clock Manager
DDR	double-data-rate
FF	Flip-Flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GBIC	Gigabit Interface Converter
Gb/s	Gigabits per second
GMII	Gigabit Media Independent Interface
HDL	Hardware Description Language
I/F	Interface
I/O	Input/Output
IES	Cadence Incisive Enterprise Simulator
IOB	Input Output Block
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mb/s	Megabits per second
MHz	Mega Hertz
MII	Media Independent Interface
PCS	Physical Coding Sublayer
PHY	physical-side interface
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
RAM	Random Access Memory
RGMII	Reduced Gigabit Media Independent Interface
Rx	Receive
SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media Independent Interface
UCF	User Constraints File
VCS	Verilog Compiled Simulator (Synopsys)
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
10/23/06	1.0	Initial Xilinx release.
2/15/07	2.0	Core updated to version 1.2; Xilinx tools 9.1i.
8/8/05	2.2	Core updated to version 1.3; Xilinx tools 9.2, IUS v5.8.
3/24/08	3.0	Core updated to version 1.4; Xilinx tools 10.1; Virtex-5 FXT FPGA support.
9/19/08	4.0	Core updated to version 1.5; Virtex-5 TXT FPGA support.
4/24/09	5.0	Core updated to version 1.6 and Xilinx tools updated to version 11.1.
4/9/10	6.0	Core updated to version 1.7 and Xilinx tools updated to version 12.1.
3/1/11	7.0	Core updated to version 1.8 and Xilinx tools updated to version 13.1.

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