LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard v2.1

DS590 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-5 FPGA RocketIO™ GTP Transceiver Wizard automates the task of creating HDL wrappers(1) to configure the high-speed serial GTP transceivers in the Virtex®-5 LXT and SXT sub-families.

The menu-driven interface allows one or more GTP transceivers to be configured using pre-defined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols. The Wizard produces a wrapper, an example design, and a test bench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Virtex-5 FPGA RocketIO GTP transceivers
- Users can configure Virtex-5 family GTP transceivers to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Included protocol templates provide support for the following specifications: Aurora 8B/10B, CPRI™, Fibre Channel 1x, Gigabit Ethernet, HD-SDI, OBSAI, OC3, OC12, OC48, PCI Express® (PCIe®) generation1, SATA 1.5 Gbps, SATA 3 Gbps, Serial RapidIO, and XAUI
- Automatically configures analog settings
- Each custom wrapper includes example design, test bench; and both implementation and simulation scripts

LogiCORE IP Facts	
Core Specifics	
Supported Device Family	Virtex-5 LXT/SXT (1)
Provided with Core	
Documentation	Product Specification Getting Started Guide
Design File Formats	Verilog and VHDL
Constraints File	.ucf (user constraints file)
Verification	Example Design and Test Bench
Instantiation Template	Verilog or VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 12.1 (2)
Verification	Mentor Graphics ModelSim® 6.5c and above
Simulation	ISim 12.1 Mentor Graphics ModelSim 6.5c and above
Synthesis	XST12.1 Synplicity Synplify Pro D-2009.12
Support	
Provided by Xilinx, Inc. at http://www.xilinx.com/support	

1. For more information on the Virtex-5 devices, see the *Virtex-5 Family Overview* [Ref 1]
2. ISE Service Packs can be downloaded from http://www.xilinx.com/support/download.htm

1. See the *LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard Getting Started Guide* [Ref 2] for an overview of the procedure to create a wrapper.

Functional Overview

Figure 1 outlines the steps required to configure GTP transceivers using the Wizard. Start the CORE Generator™ tool and select the Virtex-5 FPGA RocketIO GTP Transceiver Wizard, then follow the steps outlined in the chart to configure the transceivers and generate a wrapper that includes an accompanying example design. If an existing template is being used with no changes, click **Generate**. If modifying a standard template or starting from scratch, proceed through the Wizard and adjust the settings as needed.

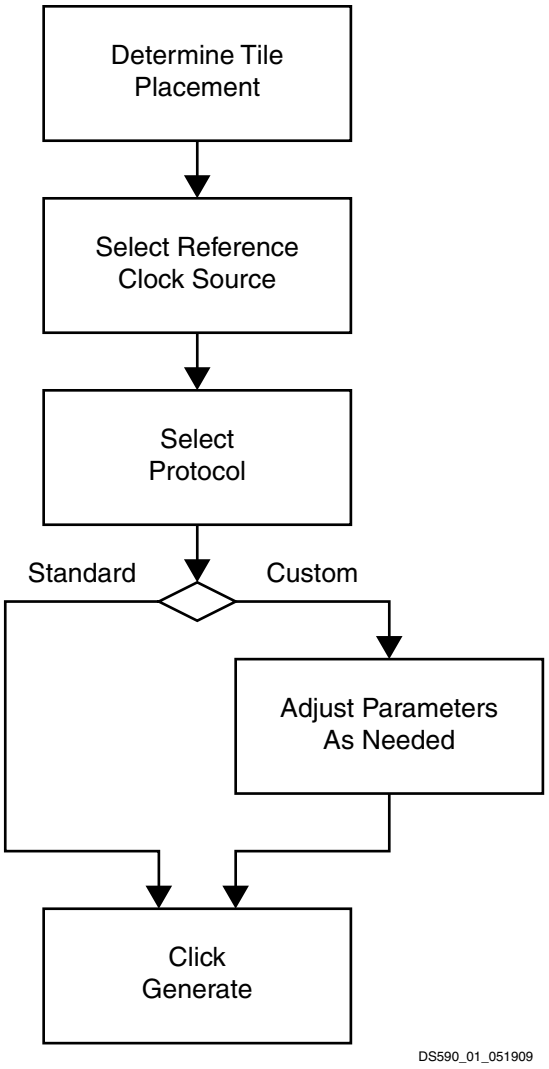

Figure 1: **GTP Wizard Configuration Steps**

See the *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* [Ref 3] for details on the features and parameters available.

Wrapper Overview

Figure 2 shows the block diagram of the wrapper, example design, and test bench produced by the Wizard.

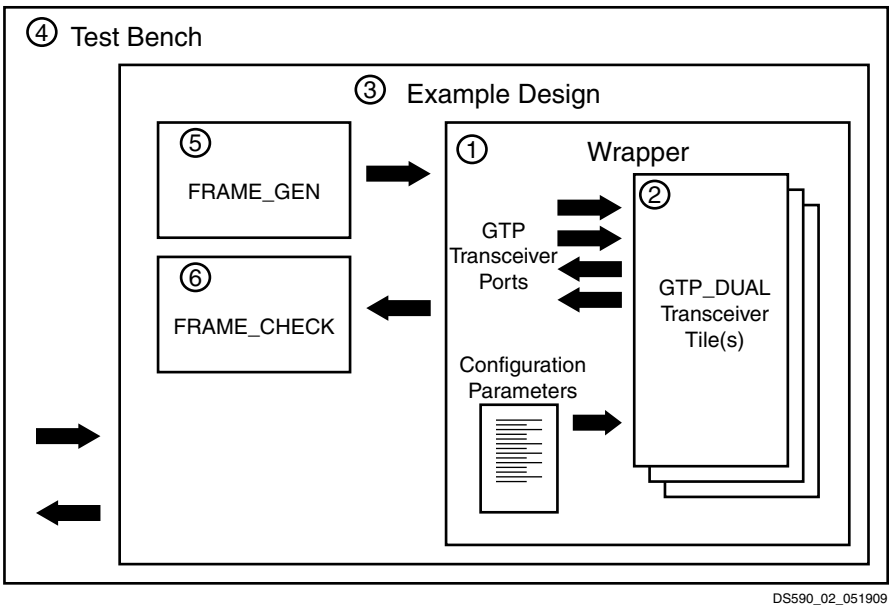

Figure 2: **Wrapper Block Diagram**

The wrapper comprises six components:

1. Wrapper: The specific GTP transceiver configuration parameters set with the Wizard.
2. GTP_DUAL Transceiver Tile(s): Instantiated tiles selected with the Wizard.
3. Example Design: Temporary top-level design that will be replaced with the actual application.
4. Test Bench: Top-level test bench to aid in simulation of the design.
5. FRAME_GEN Module: Generates a user-definable data stream for simulation analysis.
6. FRAME_CHECK Module: Tests for correct transmission of data stream for simulation analysis.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Virtex-5 FPGA RocketIO GTP Transceiver Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.1 or higher. For more information, please visit the Architecture Wizards web page. Information about additional Xilinx LogiCORE

modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. DS100: *Virtex-5 Family Overview*
2. UG188: *LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard Getting Started Guide*
3. UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
03/01/07	1.2	Initial Xilinx release. Wizard v1.4 release.
05/17/07	1.3	Wizard v1.5 release.
08/15/07	1.4	Wizard v1.6 release.
10/10/07	1.5	Wizard v1.7 release.
03/24/08	1.6	Wizard v1.8 release.
03/24/08	1.6.1	Change “test bench” to two words. Add “IP” after “LogiCORE”. Add support link. Move ISE trademark from footnote to table. Add line above copyright statement.
06/26/08	1.9	Synchronize document version with Wizard version. Revise version numbers.
06/27/08	1.9.1	Update release date and trademarks.
06/24/09	1.10	Wizard v1.10 release.
04/19/10	2.1	Wizard v2.1 release. Updated the Wizard and tool versions and the Features section. Added "Ordering Information."

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