LogiCORE IP Color Filter Array Interpolation v3.0

DS722 December 14, 2010 **Product Specification**

Introduction

The Xilinx Color Filter Array Interpolation LogiCORE™ IP provides an optimized hardware block to reconstruct sub-sampled color data for images captured by an image sensor fitted with a Bayer Color Filter Array. The color filter array overlaid on the silicon substrate enables CMOS or CCD image sensors to measure local light intensities corresponding to different wavelengths. However, the sensor measures the intensity of one principal color at any location. The Color Filter Array Interpolation LogiCORE IP provides an efficient and low-footprint solution to interpolate the missing color components for every pixel.

Features

- RGB and CMY Bayer image sensor support
- 5x5 interpolation aperture
- Low-footprint, high quality interpolation
- Support for streaming or frame buffer processing
- Selectable processor interface
  - EDK pCore
  - General Purpose Processor
  - Constant Interface
  - Transparent Interface
- 8-, 10-, and 12-bit input and output precision
- Automatic detection of timing parameters and timing signal polarities

Applications

- Pre-processing block for image sensors
- Video surveillance
- Industrial imaging
- Video conferencing
- Machine vision
- Other imaging applications

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]	Spartan®-3A DSP, Spartan-6, Virtex®-5, Virtex-6				
Supported User Interfaces	General Processor Interface, EDK PLB 4.6, Constant Interface, Transparent Interface				
	Resources[2]				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP48s**	**Block RAMs**	**Max. Freq.[3]**
Data Width=8	2616	3073	8	3(36)+ 4(18)	279.49
Data Width=10	3166	3581	8	4(36)+ 3(18)	289.44
Data Width=12	3640	4130	8	5(36)+ 2(18)	255.89
Provided with Core					
Documentation	Product Specification				
Design Files	Netlists, EDK pCore files, C drivers				
Example Design	Not Provided				
Test Bench	Not Provided				
Constraints File	Not Provided				
Simulation Models	VHDL or Verilog Structural, C, and MATLAB™				
Tested Design Tools					
Design Entry Tools	CORE Generator™ tool, Platform Studio (XPS)				
Simulation	ModelSim v6.5c, Xilinx ISim 12.4				
Synthesis Tools	XST 12.4				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.
2. Resources listed here are for Virtex-6 devices, using constant interface with maximum number of input rows and columns set to 1024. For more complete performance data, see Core Resource Utilization and Performance
3. Performance numbers listed are for Virtex-6 FPGAs. For more complete performance data, see Core Resource Utilization and Performance

General Overview

Images captured by a CMOS/CCD image sensor are monochrome in nature. To generate a color image, three primary colors (Red, Green, Blue or Cyan, Magenta, Yellow) are required for each pixel. Before the invention of color image sensors, the color image was created by superimposing three identical images with three different primary colors. These images were captured by placing different color filters in front of the sensor, allowing a certain bandwidth of the visible light to pass through.

Kodak scientist Dr. Bryce Bayer realized that an image sensor with a Color Filter Array (CFA) pattern would allow the reconstruction of all the colors of a scene from a single image capture. The color filter array is manufactured as part of the image sensor as a set of colored micro-lenses laid over the phototransistors. Example CFA patterns are shown in Figure 1. These are called Bayer patterns and are used in most digital imaging systems.

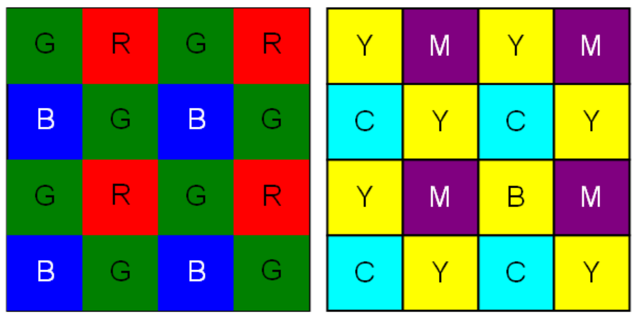

Figure 1: **RGB and CMY Bayer CFA Patterns**

The original data for each pixel only contains information about one color, depending on which color filter is positioned over that pixel. However, information for all three primary colors is needed at each pixel to reconstruct a color image. Some of the missing information can be recreated from the information available in neighboring pixels. This process of recreating the missing color information is called color interpolation or demosaicing and may require dedicated hardware to process the image data in real-time

There is no exact method to fully recover the missing information, as color channels have been physically sub-sampled by the CFA before proper low-pass filtering could take place, which leads to aliasing between color channels.

Perfect recovery of the original signal is not possible; however, the aliasing can be suppressed significantly by capitalizing on the temporal and spatial redundancies and structured nature of natural images/video sequences.

A variety of simple interpolation methods, such as Pixel Replication, Nearest Neighbor Interpolation, Bilinear Interpolation, and Bi-cubic Interpolation have been widely used for CFA demosaicing. However, simple methods usually compromise quality, and more elaborate methods require the use of an external frame buffer. The Xilinx Color Filter Array Interpolation LogiCORE IP was designed to efficiently suppress interpolation artifacts, such as the zipper and color aliasing effects, by minimizing Chrominance Variances in a 5x5 neighborhood (Figure 2).

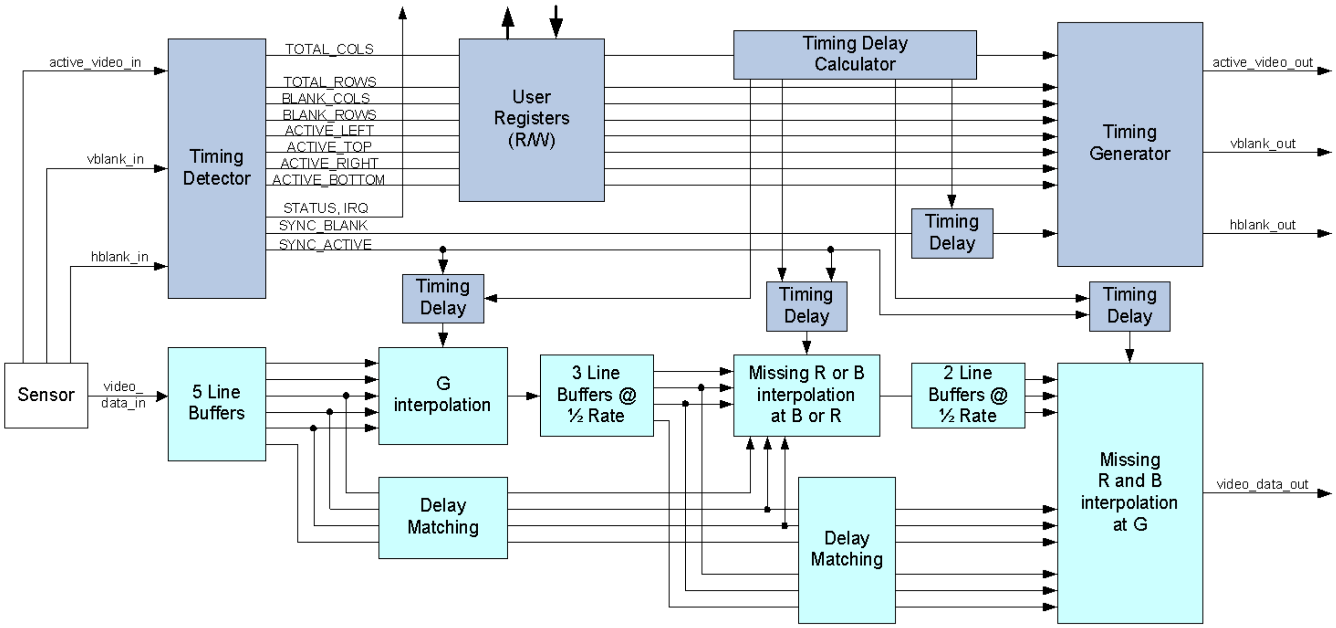

Figure 2: **Xilinx Color Filter Array Interpolation Block Diagram**

Image sensors that incorporate either Bayer RGB or CMY [Ref 1] Color Filters with all possible phase combinations are supported by the Xilinx Color Filter Array Interpolation LogiCORE IP.

The Xilinx Color Filter Array Interpolation LogiCORE IP also enables the user to couple the image sensor to downstream processing modules. The built-in timing detector module measures timing parameters of the input video stream, such as the total number of rows and columns, blank rows and columns, and makes the measurement results accessible through an EDK or general processor interface. A built-in, programmable timing generator module can create `hblank`, `vblank` and `active video` signals based on the user-provided parameters, and then use these signals to re-frame the input video data-stream. This module enables one to change the position of blanked regions as well as to crop the active area. However, the CFA Interpolation block cannot change the input/output image sizes, the input and output pixel clock rates, or the total image size.

Processor Interfaces

The Color Filter Array Interpolation core supports the following four processor interface options.

- EDK pCore Interface
- General Purpose Processor Interface
- Constant Interface
- Transparent Interface

The processor interfaces allow access to input timing information measured by the internal timing detector circuitry (Figure 2) and to control output timing signals by programming the built-in timing generator. From the edge transitions of the three input timing signals, the timing circuitry can measure:

- Blanking signal polarities
- Overall (total) frame dimensions
- The size and position of the non-blank area
- The size and position of the active area

Blanking Signal Polarities

Typical constituents of a video stream, blanking signals provide framing and blanking information that complements and formats image data provided via the `video_data_in` port. Image sensors provide this information by active high (data valid) signaling [Ref 2], or active low (blank) signaling.

The Xilinx Color Filter Array core is equipped with automatic detection of blanking signal polarity, based on the phase relations between the blanking and the active signals. The `active_video` input signal is assumed active high. If `active_video_in` is high during the logic high period of a blanking signal, that blanking signal is considered active high (valid signaling). If `active_video_in` is high during the logic low period of a blanking signal, the blanking signal is considered active low (blank signaling).

Note: **The high portion of `active_video_in` should not extend across edges of either blanking signals.**

The following definition of timing parameters assumes the `hblank_in` and `vblank_in` are driven by blanking signals, with logic high corresponding to blanked, logic low corresponding to non-blanked areas.

Definition of Timing Parameters

The periodic vblank, hblank, and `active_video` signals define the frame boundaries, as well as the blanked and active areas within a video stream. Edges of the vblank signal identify frame boundaries, and the blank/non-blank rows within frames. Edges of the hblank signal identify the blank/non-blank columns within frames, and also determine the total number of columns (`TOTAL_COLUMNS`) in the frame, which is the number of clock cycles between two rising (or falling) edges of hblank.

Note: **The Color Filter Array core supports only `hblank_in` signals that are periodic through the entire frame time.**

If the video stream signals were plotted line-by-line in a coordinate system scanning from left to right, top towards bottom, with the top-left corner identified by the falling edge of the vblank signal, the phase relationships between the vblank, hblank, and active video signals would define three rectangles: the total area containing the non-blank area, which contains the active area (Figure 3).

The timing parameters defining the sizes and positions of the total, non-blank and active areas can be defined as:

TOTAL_COLUMNS:	Defines the total number of columns, counting from 1, in a video frame. This is equal to the number of clk periods in a full hblank period.
TOTAL_ROWS:	Defines the total number of rows, counting from 1, in a video frame. This is equal to the number of hblank periods in a full vblank period.
BLANK_ROWS:	Defines the number of blank rows, counting from 1, in a video frame. This is equal to the number of hblank periods in the vertical blanking period.
BLANK_LEFT:	Defines the index, counting from 0, of the first non-blank column (on the left side of the active area).
NON_BLANK_COLUMNS	The number of clk periods, counting from 1, when hblank is inactive in a full hblank period.
BLANK_RIGHT:	Defines the index, counting from 0, of the first blank column on the right side of the active area. `BLANK_RIGHT=BLANK_LEFT+NON_BLANK_COLUMNS`
ACTIVE_TOP:	Defines the index of the first active row, where row 0 is at the beginning of the vertical non-blank period. The active area is typically smaller than the non-blank area, which for a typical sensor includes optically masked (inactive) pixels.
ACTIVE_LEFT	Defines the index, counting from 0, of the first active column. The active area is typically smaller than the non-blank area, which for a typical sensor includes optically masked (inactive) pixels.
ACTIVE_ROWS:	Number of `active_video` pulses in the vertical non-blanking period.
ACTIVE_COLUMNS:	Number of clock cycles between the rising and falling edges of `active_video`.
ACTIVE_RIGHT:	Defines the index, counting from 0, of the first non-active column on the right side of the active area. `ACTIVE_RIGHT=ACTIVE_LEFT+ACTIVE_COLUMNS`
ACTIVE_BOTTOM:	Defines the index of the first non-active row below the active area of the frame, where row 0 is at the beginning of the vertical non-blank period. `ACTIVE_BOTTOM = ACTIVE_TOP+ACTIVE_ROWS`

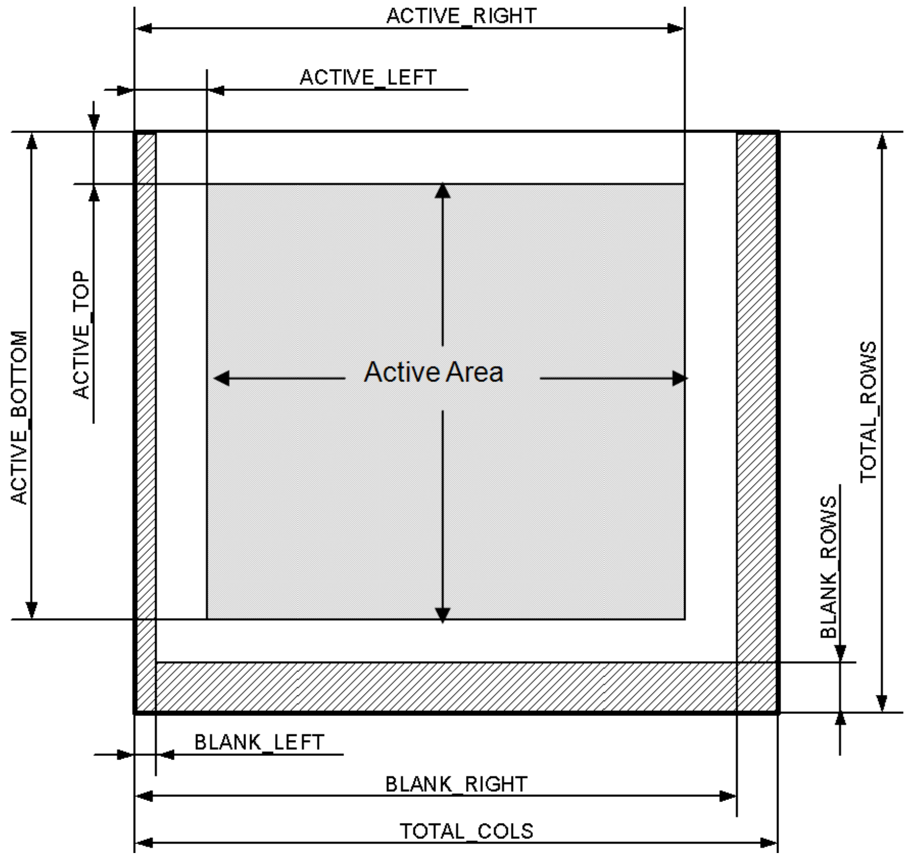

Figure 3: **Timing Parameters**

The logic high state of input signal `active_video_in` marks samples of `video_data_in` as valid. Although this signal could be used to mark an arbitrary region of the frame active, typical image sensors use this signal to designate a rectangle within the non-blank area as an active/valid area.

Note: The Color Filter Array Interpolation core only supports `active_video_in` signals that designate a rectangular area, are contiguous within one hblank period, and are periodic during the active region of the frame.

The top-left corner of the active area is defined by `ACTIVE_TOP` and `ACTIVE_LEFT`, which are the coordinates of the first sample marked active by `active_video_in` in the coordinate system defined by the blanking input signals. Similarly, `ACTIVE_BOTTOM` and `ACTIVE_RIGHT` are the coordinates of the last sample marked active by `active_video_in`. An example of horizontal timing and corresponding timing parameters is provided in Figure 4.

Timing Tolerances

Due to state-machine setup and reset constraints internal to the Xilinx Color Filter Array core, the following limitations must be observed when configuring the image sensor to be used in conjunction with the core:

- BLANK_ROWS > 2
- ACTIVE_LEFT > 3
- BLANK_LEFT <= ACTIVE_LEFT
- BLANK_LEFT + (TOTAL_COLS-BLANK_RIGHT) > 2
- ACTIVE_RIGHT < TOTAL_COLS - 5
- ACTIVE_RIGHT - ACTIVE_LEFT > 31
- BLANK_RIGHT> = ACTIVE_RIGHT
- ACTIVE_BOTTOM - ACTIVE_TOP > 31

Figure 4 shows an example in which these conditions are met.

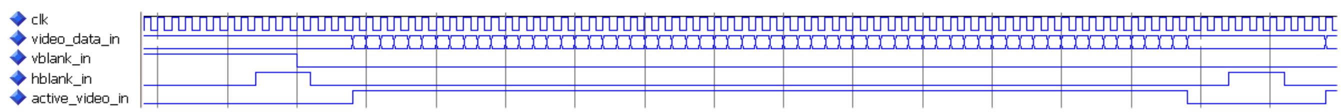

Figure 4: **Horizontal Timing Example**

In this example, the timing parameters are as follows:

BLANK_LEFT =1

(CLK cycles between a falling edge of vblank_in and the next falling edge of hblank_in)

ACTIVE_LEFT = 4

(CLK cycles between a falling edge of vblank_in and the next rising edge of active_video_in)

ACTIVE_RIGHT = 63

(CLK cycles between a falling edge of vblank_in and the next falling edge of active_video_in)

BLANK_RIGHT = 66

(CLK cycles between a falling edge of vblank_in and the next rising edge of hblank_in)

TOTAL_COLS = 70

(CLK cycles between falling edges of hblank_in)

BLANK_POLARITY_IN = 0

(Both hblank and vblank signals in this example are active-low)

The propagation delay of the Color Filter Array Interpolation core depends on actual parameterization, but is at least four full line-times. Deasserting CE suspends processing, which may be useful for data-throttling to temporarily cease processing of a video stream to match the delay of other processing components.

The example in Figure 5 illustrates vertical timing for a very short video frame.

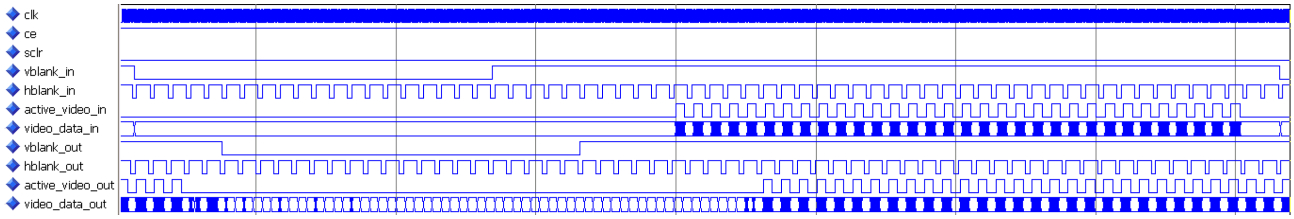

Figure 5: **Vertical Timing Example**

Timing parameters illustrated in this figure are as follows:

TOTAL_ROWS = 64

TOTAL_COLS = 64

BLANK_ROWS = 20

ACTIVE_TOP = 10

ACTIVE_BOTTOM = 42

BLANK_POLARITY_IN = 3

The non-blanked horizontal area can be flush with the active area:

(ACTIVE_LEFT = BLANK_LEFT; ACTIVE_RIGHT= BLANK_RIGHT)

Note: **If the particular image sensor targeted does not provide the `active_video` signal, a signal driving the `active_video_in` port can be created as:**

`active_video_in` = (`hblank_in` XNOR `hblank_polarity`) AND (`vblank_in` XNOR vblank_polarity)

where the `blank_polarity` signals designate whether the horizontal and vertical blanking signals are active high (1), or active low (0) as defined in Blanking Signal Polarities.

EDK pCore Interface

Many imaging applications have an embedded processor that can dynamically control the parameters in the core. The developer can select an EDK pCore interface, which creates a pCore that can be added to an EDK project as a hardware peripheral. This pCore provides a memory-mapped interface for the programmable registers in the core, which are described in Table 1.

The EDK Interface generates additional Processor Local Bus (PLB) interface ports besides the Xilinx Streaming Video Interface (XSVI), `clk`, `ce`, and `sclr` signals (Figure 12). The PLB bus signals are automatically connected when the generated pCore is inserted into an EDK project. For more information on these signals, see [Ref 3]. The XSVI is described in the Xilinx Streaming Video Interface section.

Table 1: **EDK pCore Interface Register Descriptions**

Address Offset	Read-Write	Name	Description
0x00000000	R/W	cfa_reg_00_control	General control register. Default value is 1.
0x00000004	R/W	cfa_reg_01_reset	Software reset register. Default value is 0.
0x00000008	R	cfa_reg_02_status	General status register.
0x0000000C	R/W	cfa_reg_03_interrupt_control	Interrupt control register
0x00000010	R/W	cfa_reg_04_active_left	User defined value for ACTIVE_LEFT(1)
0x00000014	R/W	cfa_reg_05_active_right	User defined value for ACTIVE_RIGHT(1)
0x00000018	R/W	cfa_reg_06_active_top	User defined value for ACTIVE_TOP(1)
0x0000001C	R/W	cfa_reg_07_active_bottom	User defined value for ACTIVE_BOTTOM(1)
0x00000020	R/W	cfa_reg_08_total_rows	User defined value for TOTAL_ROWS(1)
0x00000024	R/W	cfa_reg_09_total_cols	User defined value for TOTAL_COLS(2)
0x00000028	R/W	cfa_reg_10_blank_rows	User defined value for BLANK_ROWS(1)
0x0000002C	R/W	cfa_reg_11_blank_left	User defined value for BLANK_LEFT(1)
0x00000030	R/W	cfa_reg_12_blank_right	User defined value for BLANK_RIGHT(1)
0x00000034	R/W	cfa_reg_13_blank_polarity	User defined polarity values for Vertical (Bit 1) and Horizontal (Bit 0) Blanking. 0: indicates blanking (active low) signal 1: indicates valid video (active high) signal
0x00000038	R/W	cfa_reg_14_bayer_phase	User defined register to specify the Bayer grid. Bits 0 (bayer_phase_x) and 1 (bayer_phase_x) specify whether the top-left corner of the Bayer sampling grid starts with a Green, Red or Blue pixel.
0x0000003C	R	cfa_reg_15_active_left_r	ACTIVE_LEFT(1) value measured by the core
0x00000040	R	cfa_reg_16_active_right_r	ACTIVE_RIGHT(1) value measured by the core
0x00000044	R	cfa_reg_17_active_top_r	ACTIVE_TOP(1) value measured by the core
0x00000048	R	cfa_reg_18_active_bottom_r	ACTIVE_BOTTOM(1) value measured by the core
0x0000004C	R	cfa_reg_19_total_rows_r	TOTAL_ROWS(2) value measured by the core
0x00000050	R	cfa_reg_20_total_cols_r	TOTAL_COLS(2) value measured by the core
0x00000054	R	cfa_reg_21_blank_rows_r	BLANK_ROWS(1) value measured by the core
0x00000058	R	cfa_reg_22_blank_cols_r	BLANK_LEFT(1) value measured by the core
0x0000005C	R	cfa_reg_23_blank_cols_r	BLANK_RIGHT(1) value measured by the core
0x00000060	R	cfa_reg_24_blank_polarity_r	Measured blank polarity for Vertical (Bit 1) and Horizontal (Bit 0) Blanking. 0: indicates blanking (active low) signal 1: indicates valid video (active high) signal

1. Counting of rows and columns start from 0, that is, if the first pixel of the first line is active, both ACTIVE_LEFT and ACTIVE_TOP will be equal to 0.
2. Counting of total rows and columns starts from 1. For example, if rows 0 - 499 are non-blank, and 500-599 are blank, there are TOTAL_ROWS = 600 lines in the frame.

All of the Write registers are also readable, enabling the user to verify writes or read back current values. Default values of timing registers are defined in the Graphical User Interface (GUI).

Control Register

Table 2 contains the Control Register descriptions.

Table 2: **Control Register Description**

Bit	Name	Function
0	SW_ENABLE	Software Enable Register. '0' effectively disables the core halting further operations, which blocks the propagation of all video signals. The default value of SW enable is 1 (enabled).
1	REG_UPDATE	Host processor write done semaphore. '1' indicates the host processor has finished updating timing registers, which are ready to be copied over at the next V_SYNC signal. (See General EDK Programming Guidelines)
2	CLEAR_STAT	'1' clears flags in the status registers (clears interrupt source).

Software Reset Register

Table 3 contains the Software Reset Register descriptions.

Table 3: **Software Reset Register Description**

Bit	Name	Function
0	SW_RESET	Software Reset Register. The default value of SW_RESET is 0.

The core can be effectively reset in-system by asserting the software reset (bit 0), which returns the timing registers to their default values, specified through the GUI when the core is instantiated. The core outputs are also forced to 0 until the SW_RESET bit is deasserted.

Status Register

Table 4 provides the Status Register descriptions.

Table 4: **Status Register Descriptions**

Bit	Name	Function
0-6	-	Reserved
7	TIMING_LOCKED	'1' indicates that the timing module of the core has locked on the input timing signals and is generating stable output timing signals
8	VSYNC_DET	Vertical Sync detected
9	VSYNC_ERR	Vertical Sync error (TOTAL_ROWS larger than *MAX_ROWS* parameter)
10	HSYNC_ERR	Horizontal Sync error (*TOTAL_COLS* larger than *MAX_COLS* parameter)
11	VBLANK_CHG	VBLANK POLARITY changed since last vblank_in falling edge[(1)]
12	HBLANK_CHG	HBLANK POLARITY changed since last vblank_in falling edge[(1)]
13	TROWS_CHG	TOTAL_ROWS changed since last vblank_in falling edge[(1)]
14	TCOLS_CHG	TOTAL_COLS changed since last vblank_in falling edge[(1)]
15	BROWS_CHG	BLANK_ROWS changed since last vblank_in falling edge[(1)]
16	BCOLS_CHG	BLANK_COLS changed since last vblank_in falling edge[(1)]

1. Assumes that vblank_in is active high.

Interrupt Control Register

Table 5 provides the Control Register descriptions.

Table 5: **Interrupt Control Register Descriptions**

Bit	Name	Function
0	INT_EN	Enable/Disable Interrupts
1	CLR_SRC	Clear interrupt sources
2-7	-	Reserved
8	VSYNC_DET_INT	‘1’ enables rising VSYNC_DET to request interrupt
9	VSYNC_ERR_INT	‘1’ enables rising VSYNC_ERR to request interrupt
10	HSYNC_ERR_INT	‘1’ enables rising HSYNC_ERR to request interrupt
11	VBLANK_CHG_INT	‘1’ enables rising VBLANK_CHG to request interrupt
12	HBLANK_CHG_INT	‘1’ enables rising HBLANK_CHG to request interrupt
13	TROWS_CHG_INT	‘1’ enables rising TROWS_CHG to request interrupt
14	TCOLS_CHG_INT	‘1’ enables rising TCOLS_CHG to request interrupt
15	BROWS_CHG_INT	‘1’ enables rising BROWS_CHG to request interrupt
16	BCOLS_CHG_INT	‘1’ enables rising BCOLS_CHG to request interrupt

If multiple bits of the Interrupt Control Register are set to 1, the interrupt service routine has to determine the source of the interrupt by polling the Status Register. To facilitate subsequent interrupts by the same event, the interrupt service routine has to clear the interrupt source in the Status Register.

If multiple bits of the Interrupt Control Register are set to 1, the interrupt service routine has to determine the source of the interrupt by polling the Status Register. To facilitate subsequent interrupts by the same event, the interrupt service routine has to clear the interrupt source in the Status Register.

Timing Registers 0x0000000C - 0x00000028

Registers `ACTIVE_LEFT`, `ACTIVE_RIGHT`, `TOTAL_COLS`, and `BLANK_COLS` take unsigned integers smaller than generic core variable `MAX_CO`. For example, if `MAX_COLS` is defined as 1024, then the registers accept 10-bit unsigned integers.

Registers `ACTIVE_TOP`, `ACTIVE_BOTTOM`, `TOTAL_ROWS`, and `BLANK_ROWS` take unsigned integers smaller than generic core variable `MAX_ROWS`. For example, if `MAX_ROWS` is defined as 1024, then the registers accept 10-bit unsigned integers.

Bayer Phase Register

Bits 0 (bayer_phase_x) and 1 (bayer_phase_y) specify whether the top-left corner of the Bayer sampling grid starts with Green, Red, or Blue Pixel, according to Figure 6, which displays top-left corner of the imager sample matrix along with the Bayer Phase Register value combinations.

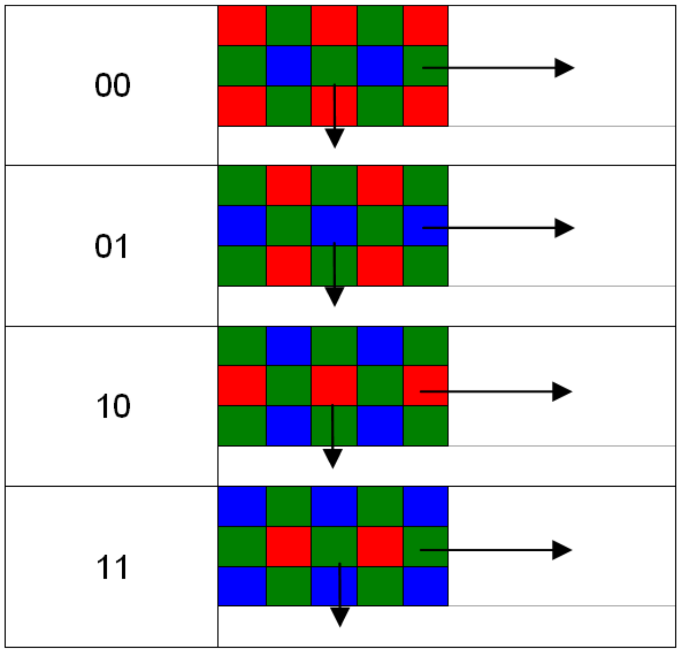

Figure 6: **Bayer Phase Register Combination Definitions**

General EDK Programming Guidelines

All registers other than control, status, and interrupt_control registers are double-buffered to ensure no image tearing happens if values are modified in the active area of a frame. Updated values for timing registers are latched into shadow registers immediately after writing, and shadow register values are copied into the working registers when vblank_in becomes inactive. Double-buffering decouples register updates from the blanking period, allowing software a much larger window to update the parameter values without tearing.

After startup/reset, output timing register values (reg_04 - reg_13), and internal registers controlling the output timing generator are constantly updated with values measured by the timing detector (reg_15 - reg_24). If the input timing changes (e.g., as a consequence of reprogramming the image sensor), the CFA core automatically adjusts its timing, which is reflected by the timing register values. However, when the user writes to any of registers reg_04 - reg_13, the core stops automatically updating reg_04 - reg_13, and retains the user-provided values. For register values not modified by the user, the core retains the values in effect at the time of the first register write. User provided values are not affecting output timing generation until the changes are committed (REG_UPDATE bit set to '1', vblank_in transitions to inactive). Subsequent changes in input timing signals will not automatically change the output timing registers (reg_04 - reg_13) signals until the core is reset.

Figure 7 provides a software flow diagram for updating registers during the operation of the core.

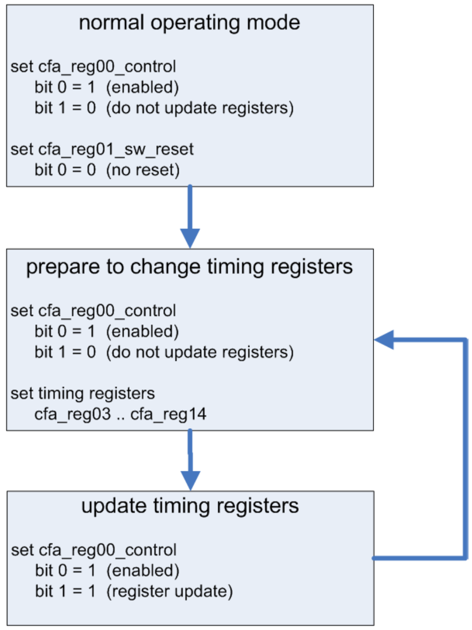

Figure 7: **Color Filter Array Interpolator Programming Flow Chart**

Programmer's Guide

The software API is provided to allow easy access to the CFA pCore's registers defined in Table 1. To utilize the API functions, the following two header files must be included in the user C code:

```
#include "cfa.h"
#include "xparameters.h"
```

The hardware settings of your system, including the base address of your CFA core, are defined in the `xparameters.h` file. The `cfa.h` file contains the macro function definitions for controlling the CFA pCore.

For examples on API function calls and integration into a user application, the drivers subdirectory of the pCore contains a file, `example.c`, in the `cfa_v3_00_a/example` subfolder. This file is a sample C program that demonstrates how to use the CFA pCore API.

EDK pCore API Functions

This section describes the functions included in the C driver (`cfa.c` and `cfa.h`) generated for the EDK pCore API.

CFA_Enable(uint32 BaseAddress);

- This macro enables a CFA instance.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`).

CFA_Disable(uint32 BaseAddress);

- This macro disables a CFA instance.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`).

CFA_Reset(uint32 BaseAddress);

- This macro resets a CFA instance. This reset affects the core immediately, and may cause image tearing. Reset affects the timing registers, forces `video_data_out` to 0, and returns timing signal outputs to their reset state until CFA_ClearReset() is called.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`)

CFA_ClearReset(uint32 BaseAddress);

- This macro clears the reset flag of the core, which allows it to re-sync with the input video stream and return to normal operation.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`).

Reading and Writing pCore Registers

Each software register defined in Table 1 has a constant defined in `cfa.h` that is set to the offset for that register. Reading a value from a register uses the base address and offset for the register:

```
Xuint32 value = CFA_ReadReg(XPAR_CFA_0_BASEADDR, CFA_REG04_ACTIVE_LEFT);
```

This macro returns the 32-bit unsigned integer value of the register. The definition of this macro is:

CFA_ReadReg(uint32 BaseAddress, uint32 RegOffset)

- Read the given register.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`).
- RegOffset is the register offset of the register (defined in Table 1).

To write to a register, use the CFA_WriteReg() function using the base address of the CFA pCore instance (from `xparameters.h`), the offset of the desired register, and the data to write. For example:

CFA_WriteReg(`XPAR_CFA_0_BASEADDR, CFA_REG04_ACTIVE_LEFT, 70`**);**

The definition of this macro is:

CFA_WriteReg(uint32 BaseAddress, uint32 RegOffset, uint32 Data)

- Write the given register.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`).
- RegOffset is the register offset of the register (defined in Table 1).
- Data is the 32-bit value to write to the register.

CFA_RegUpdateEnable(uint32 BaseAddress);

- Updating timing register values, calling RegUpdateEnable causes the CFA to start using the updated table to update on the next rising edge of `VBlank_in`. This action causes the new values written to the inactive look-up table to become the active look-up table when the `VBlank_in` rising edge occurs. The user must manually disable the register update after a sufficient amount of time to prevent continuous updates.
- This function only works when the CFA core is enabled.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`)

CFA_RegUpdateDisable(uint32 BaseAddress);

- When using a double-buffered interface, disabling the Register Update prevents the CFA correction look-up table from updating. Xilinx recommends disabling the Register Update while writing to the inactive look-up table in the CFA correction core until the write operation is complete. While disabled, writes to the inactive look up table are stored, but do not affect the core's behavior.
- This function only works when the CFA core is enabled.
- BaseAddress is the Xilinx EDK base address of the CFA core (from `xparameters.h`)

Using the Interrupt Subsystem

The Color Filter Array core can signal several exceptional events to the host processor using the `irq` output.

Bits 8-16 of the status register can request an interrupt if the interrupt enable bit corresponding to the particular status bit is set to '1'.

For example, if `TOTAL_COLS`, established by the timing detector circuitry or entered dynamically through a processor interface, gets larger than `MAX_COLS`, bit 10 of the status register is set to '1'. If bit 10 of the Interrupt Enable register is also set (='1'), and the general interrupt enable flag (Interrupt Enable Register, bit 0) is also set (='1'), then the event sets the irq output to '1' as well.

For the complete list of interrupt events, see the preceding Status Register section.

Once the interrupt is serviced by the host processor, the processor should identify the interrupt source by polling the status register, then pulsing the clear-status flag (Bit 2 of the control register). Individual interrupts sources can be masked using the Interrupt Enable Register.

General Purpose Processor Interface

The second interface option for this core is a General Purpose Processor Interface. This interface exposes the timing registers as ports enabling developers designing a system with a user-defined bus to an arbitrary processor (Table 2). The function of the registers is identical to those described in Table 1.

Double-buffering is also supported by the General Purpose Processor Interface; however the first set of registers, which are typically part of the bus decoding logic, have to be supplied by the user-defined bus interface. Values from this register bank (external to the CFA core) are copied over to the internal registers when `vblank_in` becomes inactive after the user committed the changes by setting bit 1 (`REG_UPDATE`) of the control input to '1'. Before the commit, the CFA core is using the values measured by the timing detector to generate output timing signals. The measured values can be accessed via dedicated timing outputs (see Figure 11).

Similarly, output port values reflect working register values actively used by the core. Working registers contain measurement data from the timing detector module until the user performs a successful register update which copies over input port values to the working registers.

Constant Interface

The third interface option, Constant Interface, caters to those who want to interface to a particular image sensor with known, stationary timing parameters and Bayer Phase. Once the timing parameters are established and verified, typically by inserting a prototype CFA core instance with the EDK or General Purpose Processor interface into the user design, the timing parameters can be hard coded into a CFA core with a constant interface via the CFA core GUI. The processor interface and some of the timing detector module are trimmed from the design, leading to savings in FPGA logic resources. Since there is no processor interface generated, the core is not programmable, but can be reset, enabled, or disabled using the `sclr` and `ce` pins.

Transparent Interface

The fourth and easiest to use interface option is the Transparent Interface. This interface does not require any a-priori timing information from the image sensor used other than the maximum number of rows and columns (including blank rows and columns). The built-in timing detector feeds the measured timing parameters directly to the timing generator, as if the user connected the timing output ports of the General Purpose Processor Interface to the timing input ports, in a transparent manner. However, version 3.0 of the Color Filter Array core does not contain automatic Bayer Phase detection circuitry; therefore the Bayer Phase has to be supplied through the GUI in generation time. There is no processor interface of any kind generated, and the core is not programmable but can be reset, enabled/disabled using the `sclr` and `ce` pins.

CORE Generator – Graphical User Interface

The Xilinx Color Filter Array Interpolation core is easily configured to meet the developer's specific needs through the CORE Generator™ GUI. This section provides a quick reference to parameters that can be configured at generation time. Figure 8 shows the main Color Filter Array Interpolation screen.

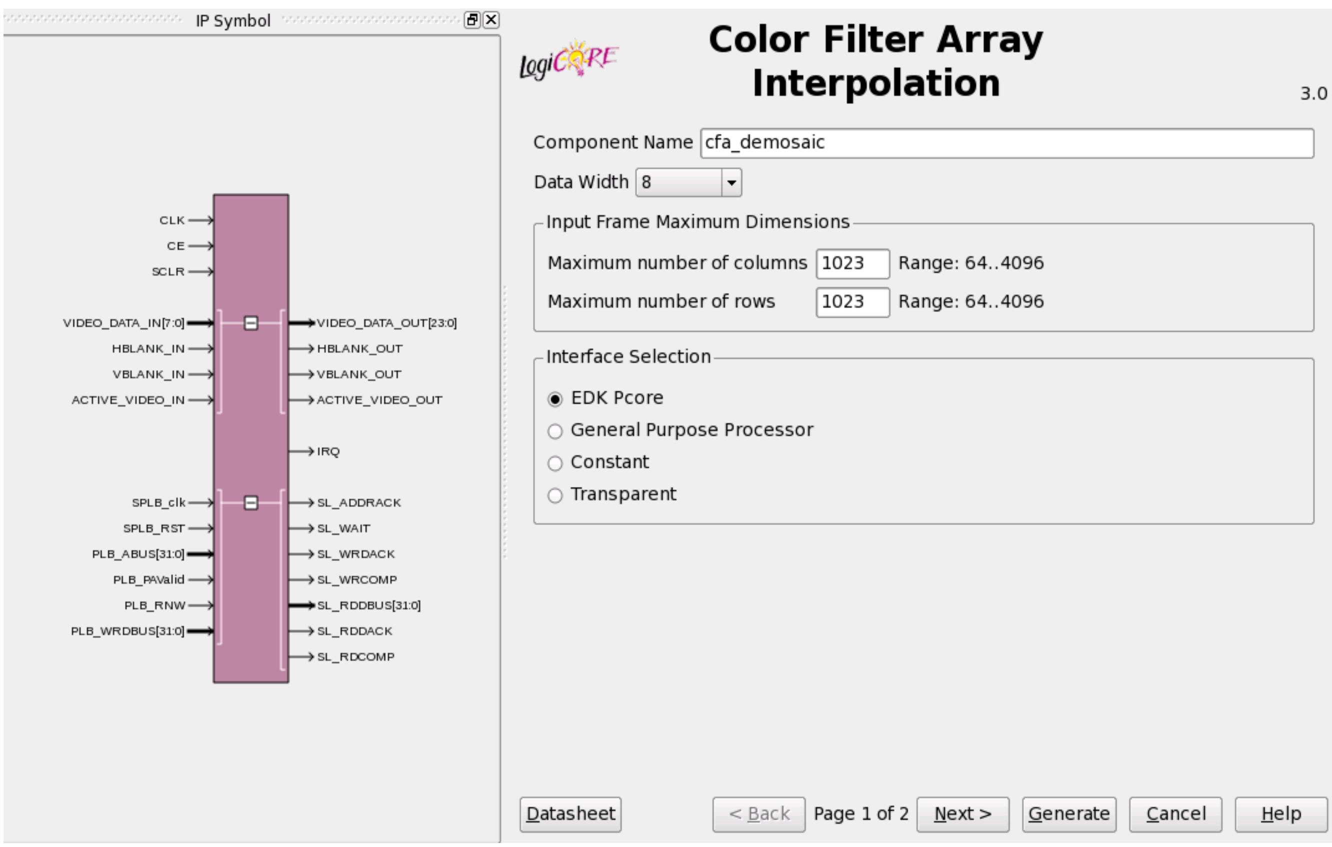

Figure 8: **Color Filter Array Interpolation Main Screen**

The GUI displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_".
- **Data Width (DWIDTH):** Specifies the bit width of input samples. Permitted values are 8, 10 and 12 bits.
- **Maximum Number of Columns (MAX_COLS)**: Specifies the maximum number of columns that can be processed by the core. Permitted values are from 128 to 4096. Specifying this value is necessary to establish the internal widths of counters and control-logic components as well as the depth of line buffers. Using a tight upper-bound on possible values of `TOTAL_COLS` results in optimal block RAM usage. However, feeding the configured CFA instance timing signals which violate the `MAX_COLS` constraint will lead to data-, and output timing signal corruption and is flagged by the status register.
- M**aximum Number of Rows (MAX_ROWS)**: Specifies the maximum number of rows that can be processed by the core. Permitted values are from 128 to 4096. Specifying this value is necessary to establish the internal widths of counters and control-logic components. Feeding the configured CFA instance timing signals which violate the `MAX_ROWS` constraint will lead to data-, and output timing signal corruption and is flagged by the status register.
- **Interface Selection:** As described in the previous sections, this option allows for the configuration of four different interfaces for the core.
  - **EDK pCore Interface**: CORE Generator software will generate a pCore which can be easily imported into an EDK project as a hardware peripheral. Internal timing measurement values can be read out, timing parameters used can be reprogrammed, and double-buffering is used to eliminate tearing of output images. See the preceding Processor Interfaces section.
  - **General Purpose Processor Interface**: CORE Generator software will generate a set of ports to be used to program the core. See the preceding Processor Interfaces section.
  - **Constant Interface**: Timing parameters provided on screen 2 of the GUI are constant, and therefore no programming is necessary. The timing detector circuitry is trimmed from the design, slightly reducing the slice-count for the core.
  - **Transparent Interface**: Timing parameters are measured automatically; therefore no programming other than setting the Bayer Phase is necessary.

The **Default Names screen (**Figure 9**)** allows for the definition of default timing, polarity, Bayer Phase and interrupt control values. For the Constant Interface, these values are permanent for the generated CFA instance. For the Transparent Interface, Timing Initialization values are discarded.

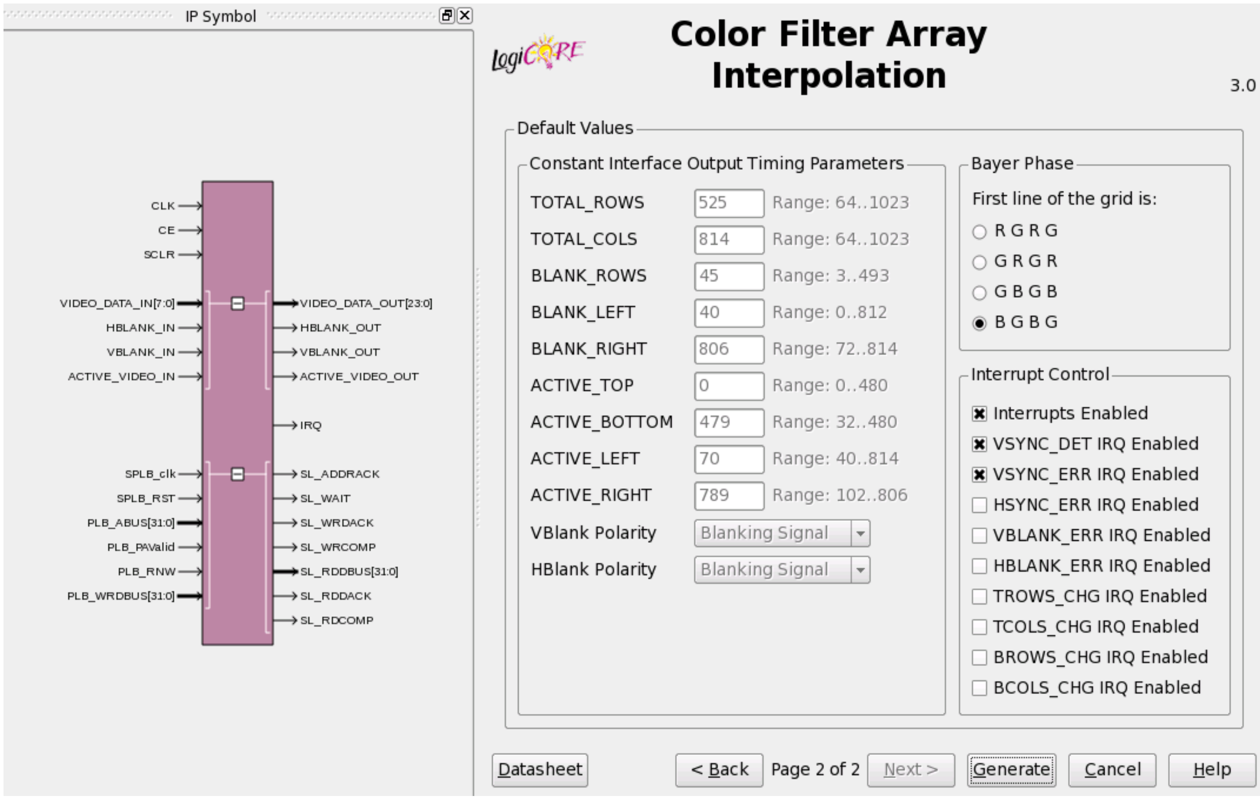

Figure 9: **Color Filter Array Interpolation, Default Status Screen**

- **Timing Initialization**: The timing initialization pane allows assigning default values for the output timing generator. This pane is only available when the Constant user interface is selected. For all other interface selections the IP core contains a timing detector module, which provides timing information for the output timing generator. This information is either directly driving the output timing generator (Transparent interface) or can be provided to a software driver, which can program the output timing generator. If the sensor-specific timing values have been established and are fixed for the core instance, the constant interface provides a way to save on resources by not instantiating a timing detector module, but using the established timing values provided though the CORE Generator GUI. For the definition of Timing Initialization generic parameters, see the preceding Definition of Timing Parameters section.
- **Bayer Phase**: Based on the data sheet of the particular image sensor used, and the particular register settings of the sensor, the user has to identify where the top-left corner of total area falls on the CFA matrix. For the first two samples, four combinations are possible. For RGB sensors, these are RG, GR, BG, GB. For CMY sensors the combinations are MY, YM, CY, YC.

Core Symbol and Port Descriptions

As discussed previously, the Color Filter Array Interpolation core can be configured with four different interface options, each resulting in a slightly different set of ports. The core uses a set of signals that is common to all of the Xilinx Video IP cores called the Xilinx Streaming Video Interface (XSVI). The XSVI signals are common to all interface options and are shown in Figure 10 and described by Table 6.

Xilinx Streaming Video Interface

The Xilinx Streaming Video Interface (XSVI) is a set of signals common to all of the Xilinx video cores used to stream video data between IP cores. XSVI is also defined as an Embedded Development Kit (EDK) bus type so that the tool can automatically create input and output connections to the core. This definition is embedded in the pCORE interface provided with the IP, and it allows an easy way to cascade connections of Xilinx Video Cores. The Color Filter Array Interpolation core uses the following subset of the XSVI signals:

- `video_data`
- `vblank`
- `hblank`
- `active_video`

Other XSVI signals on the XSVI input bus, such as `video_clk`, `vsync`, `hsync`, `field_id`, and `active_chr` do not affect the function of this core.

Note: These signals are neither propagated, nor driven on the XSVI output of this core.

The following is an example EDK Microprocessor Peripheral Definition (.MPD) file definition. DWIDTH is the value you selected when you generated the IP in CORE Generator (i.e., 8, 10, or 12).

Input Side:

```
BUS_INTERFACE BUS = XSVI_CFA_IN, BUS_STD = XSVI, BUS_TYPE = TARGET

PORT active_video_in   = active_video,                  BUS = XSVI_CFA_IN, DIR = IN
PORT hblank_in         = hblank,                        BUS = XSVI_CFA_IN, DIR = IN
PORT vblank_in         = vblank,                        BUS = XSVI_CFA_IN, DIR = IN
PORT video_data_in     = video_data, VEC=[0:(DWIDTH-1)], BUS = XSVI_CFA_IN, DIR = IN
```

Output Side:

```
BUS_INTERFACE BUS = XSVI_CFA_OUT, BUS_STD = XSVI, BUS_TYPE = INITIATOR

PORT active_video_out = active_video,                   BUS = XSVI_CFA_OUT, DIR = OUT
PORT hblank_out       = hblank,                         BUS = XSVI_CFA_OUT, DIR = OUT
PORT vblank_out       = vblank,                         BUS = XSVI_CFA_OUT, DIR = OUT
PORT video_data_out   = video_data,VEC=[0:((DWIDTH*3)-1)],BUS = XSVI_CFA_OUT, DIR=OUT
```

The Color Filter Array Interpolation IP core is fully synchronous to the core clock, clk. Consequently, the input XSVI bus is expected to be synchronous to the input clock, clk. Similarly, to avoid clock resampling issues, the output XSVI bus for this IP is synchronous to the core clock, clk. The `video_clk` signals of the input and output XSVI buses are not used.

Constant Interface

This interface does not provide additional programmability, the Constant Interface has no ports other than the Xilinx Streaming Video Interface, `clk`, `ce`, `sclr`, and `irq` signals. The Constant Interface Core Symbol is shown in Figure 10.

The Constant Interface option caters to those who want to interface to a particular image sensor with known, stationary timing parameters and Bayer Phase. Once the timing parameters are established and verified, typically by inserting a prototype CFA core instance with the EDK or General Purpose Processor interface into the user design, the timing parameters can be hard coded into a CFA core with a constant interface via the CFA core GUI. The processor interface and some of the timing detector module are trimmed from the design, leading to savings in FPGA logic resources. Since there is no processor interface generated, the core is not programmable, but can be reset, enabled, or disabled using the `sclr` and `ce` pins. The timing parameter values can be measured either by using a Color Filter Array Interpolation IP Core instance with a processor interface, or captured from the data-sheet of the image sensor. For more information on the definition of timing parameters, see Definition of Timing Parameters.

Transparent Interface

This interface option is the easiest to use and is recommended for the user who is not interested in reading out or modifying the timing parameters. This interface does not require any timing information from the image sensor used. The built-in timing detector feeds the measured timing parameters directly to the timing generator, as if the user connected the timing output ports of the General Purpose Processor Interface to the timing input ports, in a transparent manner. The Transparent Interface has no ports other than the Xilinx Streaming Video Interface, clk, ce, sclr, and irq signals. The Constant Interface Core Symbol is shown in Figure 10.

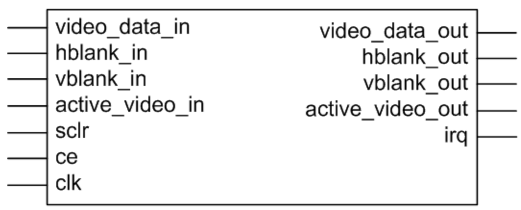

Figure 10: **Core Symbol for Constant and Transparent Interfaces**

Table 6: **Port Descriptions for the Constant and Transparent Interfaces**

Port Name	Port Width	Direction	Description
video_data_in	DWIDTH	IN	data input bus
hblank_in	1	IN	horizontal blanking input
vblank_in	1	IN	vertical blanking input
active_video_in	1	IN	active video signal input
video_data_out	3* DWIDTH	OUT	data output bus
hblank_out	1	OUT	horizontal blanking output
vblank_out	1	OUT	vertical blanking output
active_video_out	1	OUT	active video signal output
irq	1	OUT	interrupt request pin
clk	1	IN	rising-edge clock
ce	1	IN	clock enable (active high)
sclr	1	IN	synchronous clear – reset (active high)

- **video_data_in**: This is the sample input bus for Bayer patterned data. DWIDTH bits wide color values are expected in unsigned integer representation.
- **hblank_in**. This signal conveys information about the blank/non-blank regions of video scan lines.
- **vblank_in:** This signal conveys information about the blank/non-blank regions of video frames.
- **active_video_in**: This signal is high when valid data is presented at the input.
- **clk - clock:** Master clock in the design, synchronous to, or identical with video clk.
- **ce - clock enable**: Pulling `CE` low suspends all operations within the core. Outputs are held, no input signals are sampled, except for reset (`SCLR` takes precedence over `CE`).
- **sclr - synchronous clear:** Pulling `SCLR` high results in resetting all output pins to zero. Internal registers within the XtremeDSP™ slice and D-flip-flops are cleared. However, the core uses SRL16/SRL32-based delay lines for `hblank`, `vblank`, and `active_video` generation, which are not cleared by `SCLR`. This may result in non-zero outputs after `SCLR` is deasserted, until the contents of SRL16/SRL32s are flushed. Unwanted results can be avoided if `SCLR` is held active until SRL16/SRL32s are flushed.
- **video_data_out:** This bus contains RGB output in the same order as `video_data_in`. Color values are represented as DWIDTH bits wide unsigned integers.

Bits	3DWIDTH-1:2DWIDTH	2DWIDTH-1:DWIDTH	DWIDTH-1:0
video data signals	Red/Magenta	Blue/Cyan	Green/Yellow

- **hblank_out, vblank_out and active_video_out:** The corresponding input signals are delayed so `active_video` and blanking outputs are in phase with the video data output, maintaining the integrity of the video stream. The `active_video_out` signal is high when valid data is presented at the output.
- **irq:** The Interrupt output pin can be used in a processor system to signal special conditions detected by the CFA core. For more information on interrupt subsystems, see Using the Interrupt Subsystem. For a complete list of events that can be monitored, see Interrupt Control Register.

General Purpose Processor Interface

Figure 11 shows the core pinout for the General Purpose Processor Interface; Table 7 provides descriptions for its pins in addition to the pins defined in Table 6.

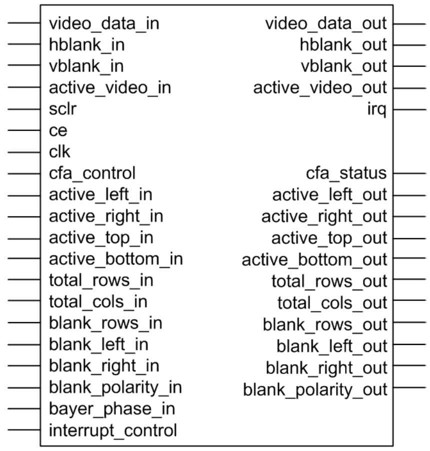

Figure 11: **Core Pinout for General Purpose Processor Interface**

Table 7: **Optional Pins for the General Purpose Processor Interface**

Port Name	Port Width	Direction	Description
control	4	IN	Bit 0: Software Enable Register Bit 1: Host processor write done semaphore Bit 2: Clear status registers (clears interrupt source) Bit 3: Reserved
status	18	OUT	Status Register
active_left_in	COLS_WIDTH	IN	User defined value for ACTIVE_LEFT[1]
active_right_in	COLS_WIDTH	IN	User defined value for ACTIVE_RIGHT[1]
active_top_in	ROWS_WIDTH	IN	User defined value for ACTIVE_TOP[1]
active_bottom_in	ROWS_WIDTH	IN	User defined value for ACTIVE_BOTTOM[1]
total_rows_in	COLS_WIDTH	IN	User defined value for TOTAL_ROWS[1]
total_cols_in	COLS_WIDTH	IN	User defined value for TOTAL_COLS[1]
blank_rows_in	ROWS_WIDTH	IN	User defined value for BLANK_ROWS[1]
blank_left_in	COLS_WIDTH	IN	User defined value for BLANK_LEFT[1]
blank_right_in	COLS_WIDTH	IN	User defined value for BLANK_RIGHT[1]
blank_polarity_in	2	IN	User defined input timing blank polarities for Vertical (Bit 1) and Horizontal (Bit 0) Blanking 0: indicates blanking (active low) signal 1: indicates valid video (active high) signal
bayer_phase	2	IN	See Bayer Phase Register
interrupt_control	17	IN	See section Using the interrupt subsystem
active_left_out	COLS_WIDTH	OUT	Input timing value measured for ACTIVE_LEFT*
active_right_out	COLS_WIDTH	OUT	Input timing value measured for ACTIVE_RIGHT[1]
active_top_out	ROWS_WIDTH	OUT	Input timing value measured for ACTIVE_TOP[1]

Table 7: **Optional Pins for the General Purpose Processor Interface *(Cont'd)***

active_bottom_out	ROWS_WIDTH	OUT	Input timing value measured for ACTIVE_BOTTOM(1)
total_rows_out	COLS_WIDTH	OUT	Input timing value measured for TOTAL_ROWS(1)
total_cols_out	COLS_WIDTH	OUT	Input timing value measured for TOTAL_COLS(1)
blank_rows_out	ROWS_WIDTH	OUT	Input timing value measured for BLANK_ROWS(1)
blank_left_out	COLS_WIDTH	OUT	Input timing value measured for BLANK_LEFT(1)
blank_right_out	COLS_WIDTH	OUT	Input timing value measured for BLANK_RIGHT(1)
blank_polarity_out	2	OUT	User defined output timing blank polarities for Vertical (Bit 1) and Horizontal (Bit 0) Blanking 0: indicates blanking (active low) signal 1: indicates valid video (active high) signal

1. See Definition of Timing Parameters, page 4
2. See Blanking Signal Polarities, page 4

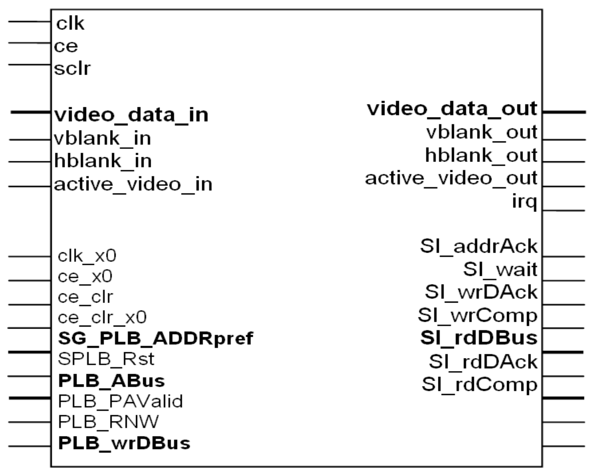

Figure 12: **Core Pinout for the EDK Processor Interface**

Quality Measures

Table 8 provides Peak Signal to Noise Ratio (PSNR) measurement results for typical test images, using 8-bit input data.

Table 8: **PSNR Results for Typical Test Images**

Image	PSNR [dB]
	34.051
	39.404
	33.736

Core Resource Utilization and Performance

For an accurate measure of the usage of primitives, slices, and CLBs for a particular instance, check the **Display Core Viewer after Generation** option in CORE Generator GUI.

The information in Table 9 and Figure 12 provides guidelines for the resource utilization of the Color Filter Array Interpolation core for typical Standard Definition (SD) and High Definition (HD) sensors with 8, 10, and 12-bit input resolutions for Spartan®-3A DSP, Spartan-6, Virtex®-5, and Virtex-6 FPGA families. This core does not use any dedicated I/O or CLK resources. The design was tested using Xilinx ISE® v12.4 tools with default tool options for characterization data.

Table 9: **SD Resolution - Maximum Resolution: 1024 Rows x 1024 Columns**

Spartan-3A DSP XC3SD3400A,FG676,-5 Speedfile: (PRODUCTION 1.33 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM16WERs**		**Clock Freq**
8	3196	3120	2563	8	10		154.61
10	3622	3477	2716	8	11		153.61
12	4327	4160	3442	8	12		155.55
Spartan-6 XC6SLX150,FGG676,C,-2 Speedfile: (PRODUCTION 1.13b 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM16**	**BRAM8**	**Clock Freq**
8	3280	2619	1031	8	10	2	172.21
10	3697	3084	1115	8	12	1	159.13
12	4256	3405	1377	8	12	2	161.34
Virtex-5 XC5VSX50T,FF665,-1 Speedfile: (PRODUCTION 1.72 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM18s**	**BRAM36**	**Clock Freq**
8	3099	2755	1208	8	4	3	230.10
10	3627	3312	1432	8	3	4	230.95
12	4188	3823	1490	8	2	5	287.19
Virtex-6 XC6VSX315T,FF1156,C,-1 Speedfile: (PRODUCTION 1.11c 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM18s**	**BRAM36**	**Clock Freq**
8	3073	2616	826	8	4	3	279.49
10	3581	3166	1019	8	3	4	289.44
12	4130	3640	1070	8	2	5	255.89

Table 10: **HD Resolution - Maximum Resolution: 2200 Rows x 2200 Columns**

Spartan-3A DSP XC3SD3400A,CS484,-4 Speedfile: (PRODUCTION 1.33 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM16WERs**		**Clock Freq**
8	3234	3156	2313	8	24		152.74
10	3661	3451	2945	8	30		154.82
12	4232	3956	3035	8	34		152.42
Spartan-6 XC6SLX150,FGG676,C,-2 Speedfile: (PRODUCTION 1.13b 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM16s**	**BRAM8s**	**Clock Freq**
8	3309	2821	1090	8	26	0	163.96
10	3715	3139	1221	8	30	2	161.19
12	4463	3776	1434	8	36	0	168.49
Virtex-5 XC5VSX50T,FF665,-1 Speedfile: (PRODUCTION 1.72 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM18s**	**BRAM36s**	**Clock Freq**
8	3243	3022	1265	8	7	8	227.48
10	3776	3663	1323	8	6	11	233.10
12	4232	3988	1525	8	6	13	245.04
Virtex-6 XC6VSX315T,FF1156,C,-1 Speedfile: (PRODUCTION 1.11c 2010-11-01)							
Data Width	**FFs**	**LUTs**	**Slices**	**DSP48s**	**BRAM18s**	**BRAM36s**	**Clock Freq**
8	3123	2754	875	8	7	8	288.27
10	3751	3487	1125	8	6	11	278.71
12	4180	3823	1248	8	6	13	267.17

References

1. Eastman Kodak Company: KAC – 1310, 1280 x 1024 SXGA CMOS Image Sensor Technical Data.
2. Aptina MT9P031: 1/2.5-Inch 5Mp Digital Image Sensor Features.
3. PLB Interface Documentation

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY.*

License Options

The Color Filter Array Interpolation core provides the following three licensing options:

- Simulation Only
- Full System Hardware Evaluation
- Full

After installing the required Xilinx ISE software and IP Service Packs, choose a license option.

Simulation Only

The Simulation Only Evaluation license key is provided with the Xilinx CORE Generator tool. This key lets you assess core functionality with either the example design provided with the Color Filter Array Interpolation core, or alongside your own design and demonstrates the various interfaces to the core in simulation. (Functional simulation is supported by a dynamically generated HDL structural model.)

No action is required to obtain the Simulation Only Evaluation license key; it is provided by default with the Xilinx CORE Generator software.

Full System Hardware Evaluation

The Full System Hardware Evaluation license is available at no cost and lets you fully integrate the core into an FPGA design, place-and-route the design, evaluate timing, and perform functional simulation of the Color Filter Array Interpolation core using the example design and demonstration test bench provided with the core.

In addition, the license key lets you generate a bitstream from the placed and routed design, which can then be downloaded to a supported device and tested in hardware. The core can be tested in the target device for a limited time before timing out (ceasing to function), at which time it can be reactivated by reconfiguring the device.

To obtain a Full System Hardware Evaluation license, do the following:

1. Navigate to the product page for this core.
2. Click Evaluate.
3. Follow the instructions to install the required Xilinx ISE software and IP Service Packs.

Full

The Full license key is available when you purchase the core and provides full access to all core functionality both in simulation and in hardware, including:

- Functional simulation support
- Full implementation support including place and route and bitstream generation
- Full functionality in the programmed device with no time outs

To obtain a Full license key, you must purchase a license for the core. Click on the "Order" link on the Xilinx.com IP core product page for information on purchasing a license for this core. After doing so, click the "How do I generate a license key to activate this core?" link on the Xilinx.com IP core product page for further instructions.

Installing Your License File

The Simulation Only Evaluation license key is provided with the ISE CORE Generator system and does not require installation of an additional license file. For the Full System Hardware Evaluation license and the Full license, an email will be sent to you containing instructions for installing your license file. Additional details about IP license key installation can be found in the ISE Design Suite Installation, Licensing and Release Notes document. any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The Color Filter Array Interpolation core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator system v12.4 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

A simulation evaluation license for the core is shipped with the CORE Generator system. To access the full functionality of the core, including FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, please visit the Color Filter Array Interpolation product page.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/24/09	1.0	Initial Xilinx release.
07/23/10	2.0	Updated with Core Version 2.0 information.
12/14/10	3.0	Updated with Core Version 3.0 information.

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