LogiCORE IP SMPTE 2022-1/2 Video over IP Receiver v1.0

Product Guide for Vivado Design Suite

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Introduction

The Xilinx LogiCORE™ IP SMPTE 2022-1/2 Video over IP Receiver core is used for broadcast applications that require bridging between constant bit rate MPEG-2 transport streams and 1 Gb/s IP networks. The module can recover IP packets lost due to network transmission errors and ensure integrity of transport streams. This core is used for developing Internet Protocol–based systems that reduce the overall cost of distribution and routing of audio and video data.

Features

- Up to 16 channels of CBR MPEG-2 transport streams in accordance with SMPTE 2022-2
- Per-channel forward error correction (FEC) in accordance with SMPTE 2022-1
- Level A and Level B FEC operations
- Block-aligned and non-block-aligned FEC operations support
- Virtual Local Area Network (VLAN) support
- AXI4-Stream data interfaces
- AXI4-Lite control interface
- Configurable channel selection based on IP source address, IP destination address, User Datagram Protocol (UDP) source port, UDP destination port, Real-time Transport Protocol (RTP) Synchronization Source (SSRC) identifier, and VLAN tag control information
- Seamless switching

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq-7000®, Virtex-7®, Kintex-7®, Artix-7®
Supported User Interfaces	AXI4-Lite, AXI4-Stream, AXI-4
Resources	See Table 2-1 through Table 2-4
Provided with Core	
Design Files	Encrypted HDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Encrypted RTL
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported devices, see Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

As broadcast and communications markets converge, broadcasters and telecommunication companies increasingly use IP networks for video stream transport. Xilinx devices bridge the broadcast and the communications industries by providing highly integrated real-time video interfaces that help broadcasters reduce costs and the time it takes to acquire, edit, and produce content.

Now that video can be delivered reliably over Ethernet, broadcasters can replace expensive mobile infrastructures that support outside live broadcasts, as well as enable remote production from existing fixed studios. This dramatically reduces both capital expenditure and operating expenses. As a result, using Ethernet to transmit multiple compressed media streams is a major customer requirement. The industry implements primarily the SMPTE 2022 set of standards to create an open and interoperable way to transmit video over Ethernet, ensure quality of service (QoS), and minimize packet loss.

As shown in Figure 1-1, SMPTE 2022-1/2 receiver core primarily targets distribution networks where multiple transport streams are carried over 1 Gb/s Ethernet networks. The core includes Forward Error Correction (FEC), which protects transport streams over IP

networks. With FEC, the receiver adds systematically generated redundant data that allows the receiver to detect and correct a limited number of packet errors.

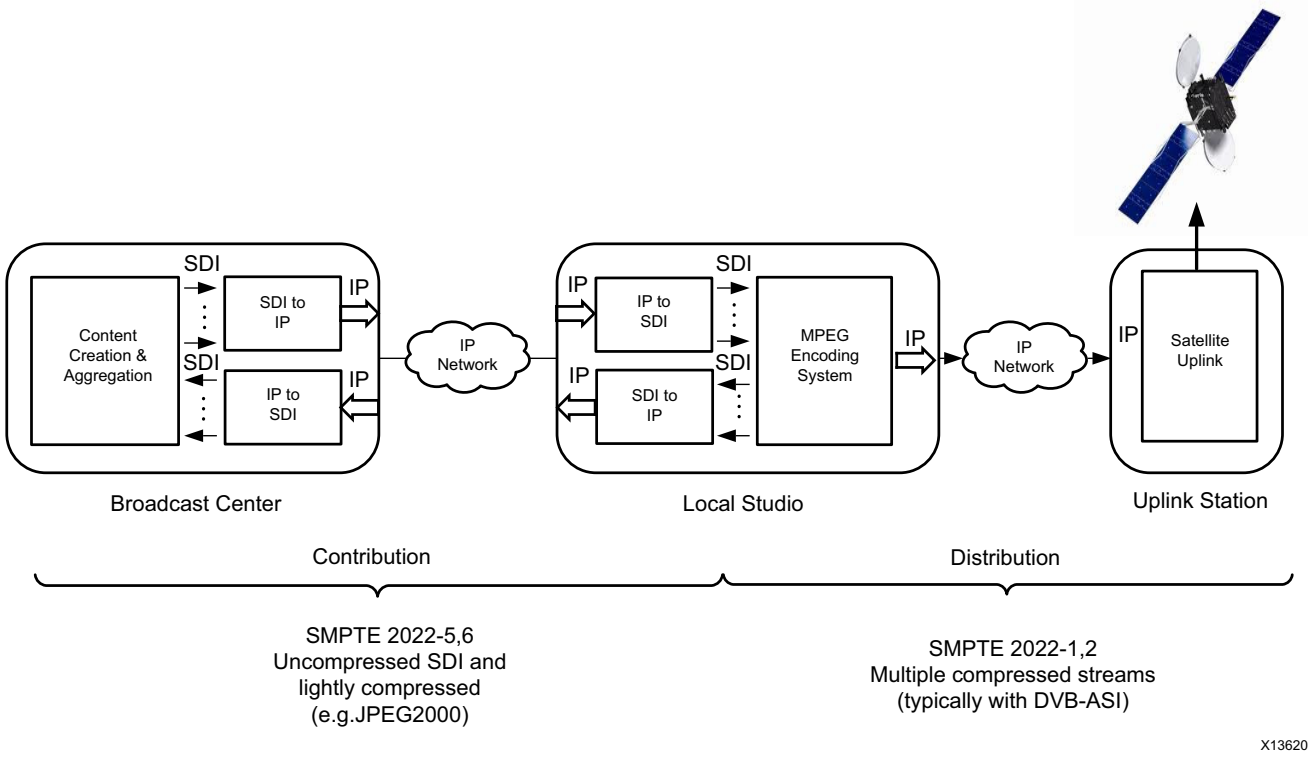

Figure 1-1: **SMPTE 2022-1/2 in Distribution Networks**

Video packets are lost for a variety of reasons, including thermal noise, storage system defects, and transmission noise introduced by the environment. FEC enables the receiver to correct these errors without using a reverse channel to request retransmission, which is not feasible in real-time systems because the latency is too great.

Feature Summary

The core de-capsulates Ethernet packets into transport streams and can recover IP packets lost because of network transmission errors, ensuring the data integrity of MPEG transport streams. The core operates seamlessly when receiving and filtering VLAN tagged Ethernet packets.

You configure and instantiate the core by using the Vivado® design tools. Core functionality is controlled through registers via an AXI4-Lite interface.

Applications

- Transport compressed constant bit rate MPEG-2 transport streams over IP networks.
- Support real-time audio/video applications in primary distribution.

Licensing and Ordering Information

This Vivado® Design Suite IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, see the SMPTE 2022-1/2 Video over IP product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado design tools have several license check points for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado design tools: Vivado Synthesis, Vivado Implementation, write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Product Specification

Standards

The SMPTE 2022-1/2 Video over IP Receiver core is compliant with the AXI4, AXI4-Stream and AXI4-Lite interconnect standards. See the Video IP: AXI Feature Adoption section of the *AXI Reference Guide* (UG761) [Ref 1] for additional information. The function of the core is compliant with SMPTE 2022-1/2.

Performance

Maximum Frequencies

The maximum achievable clock frequency and all resource counts can be affected by other tool options, additional logic in the FPGA device, different versions of Xilinx tools, and other factors. See Table 2-1 through Table 2-4 for device family–specific information.

Resource Utilization

Resources required for this core have been estimated for Zynq®-7000, Virtex-7®, Kintex-7®, and Artix®-7 devices. These values were generated using Xilinx Vivado® Design Suite. They are derived from post-synthesis reports, and might change during MAP and PAR.

Zynq-7000 Devices

Table 2-1 provides approximate resource counts for the various core options on Zynq-7000 devices.

Table 2-1: **Resource Utilization for Zynq-7000 Devices (xc7z045 Speed -1)**

CHANNEL	FEC INCLUDE	HITLESS INCLUDE	FFs	LUTs	Slices	LUT FF Pairs	36k BRAMs	18k BRAMs	DSP48E1s	Fmax (Mhz)
1	0	0	7007	3506	2154	6237	11	0	0	304
4	0	0	17309	9212	5779	15804	29	0	0	288
8	0	0	31026	15903	10978	28245	53	0	0	250
16	0	0	58460	29836	18282	51434	101	0	0	242
1	1	0	10912	5631	3462	9770	25	1	0	281
4	1	0	21211	11491	6880	19302	55	1	0	242
8	1	0	36034	18811	11933	32278	95	1	0	212
16	1	0	65629	33721	17370	55547	175	1	0	204
1	0	1	9571	4199	2950	8209	15	0	0	288
4	0	1	24975	10993	8648	21826	33	0	0	266
8	0	1	45489	19006	12805	37197	57	0	0	258
16	0	1	86500	35002	25345	71324	105	0	0	234
1	1	1	13876	6514	4055	11741	29	1	0	274
4	1	1	29669	13632	8777	25079	59	1	0	242
8	1	1	51973	22655	15445	43723	99	1	0	234
16	1	1	96567	41714	25351	78349	179	1	0	188

Virtex-7 FPGAs

Table 2-2 provides approximate resource counts for the various core options on Virtex-7 FPGAs.

Table 2-2: **Resource Utilization for Virtex-7 FPGAs (xcv7vx690t Speed -1)**

CHANNEL	FEC INCLUDE	HITLESS INCLUDE	FFs	LUTs	Slices	LUT FF Pairs	36k BRAMs	18k BRAMs	DSP48E1s	Fmax (Mhz)
1	0	0	7007	3506	2489	6517	11	0	0	304
4	0	0	17293	9198	7166	16736	29	0	0	281
8	0	0	31010	16056	9717	27113	53	0	0	242
16	0	0	58460	29844	18412	51993	101	0	0	234
1	1	0	10928	5641	3277	9608	25	1	0	274
4	1	0	21211	11499	7407	19728	55	1	0	250
8	1	0	36012	18483	11613	32138	95	1	0	219

Table 2-2: **Resource Utilization for Virtex-7 FPGAs (xcv7vx690t Speed -1) *(Cont'd)***

CHANNEL	FEC INCLUDE	HITLESS INCLUDE	FFs	LUTs	Slices	LUT FF Pairs	36k BRAMs	18k BRAMs	DSP48E1s	Fmax (Mhz)
16	1	0	65629	33722	19761	57961	175	1	0	212
1	0	1	9571	4197	2841	8164	15	0	0	288
4	0	1	24994	10968	7381	21081	33	0	0	274
8	0	1	45489	19002	12907	37187	57	0	0	258
16	0	1	86521	35004	25338	71664	105	0	0	234
1	1	1	13895	6523	4102	11980	29	1	0	274
4	1	1	29650	13620	9545	26077	59	1	0	250
8	1	1	51973	22662	15422	43661	99	1	0	219
16	1	1	96567	41714	28936	81843	179	1	0	204

Kintex-7 FPGAs

Table 2-3 provides approximate resource counts for the various core options on Kintex-7 FPGAs.

Table 2-3: **Resource Utilization for Kirtex-7 FPGAs (xc7k325t Speed -1)**

CHANNEL	FEC INCLUDE	HITLESS INCLUDE	FFs	LUTs	Slices	LUT FF Pairs	36k BRAMs	18k BRAMs	DSP48E1s	Fmax (Mhz)
1	0	0	6991	3493	2219	6247	11	0	0	288
4	0	0	17309	9210	5406	15458	29	0	0	266
8	0	0	31010	16059	10399	27865	53	0	0	242
16	0	0	58449	29409	17974	51182	101	0	0	219
1	1	0	10928	5638	3379	9739	25	1	0	274
4	1	0	21211	11494	6857	19053	55	1	0	258
8	1	0	36012	18480	11425	31903	95	1	0	219
16	1	0	65629	33722	20424	58369	175	1	0	196
1	0	1	9571	4194	2966	8309	15	0	0	296
4	0	1	24994	10964	6957	20830	33	0	0	258
8	0	1	45489	19000	14569	38308	57	0	0	234
16	0	1	86521	35006	25290	71142	105	0	0	226
1	1	1	13876	6515	4145	11869	29	1	0	266
4	1	1	29650	13620	9108	25671	59	1	0	242
8	1	1	51954	22407	15283	43267	99	1	0	219
16	1	1	96666	41480	28053	80508	179	1	0	156

Artix-7 FPGAs

Table 2-4 provides approximate resource counts for the various core options on Artix-7 FPGAs.

Table 2-4: **Resource Utilization for Artix-7 FPGAs (xc7a200t Speed -1)**

CHANNEL	FEC INCLUDE	HITLESS INCLUDE	FFs	LUTs	Slices	LUT FF Pairs	36k BRAMs	18k BRAMs	DSP48E1s	Fmax (Mhz)
1	0	0	7007	3504	2317	6341	11	0	0	204
4	0	0	17293	9195	5641	15772	29	0	0	180
8	0	0	31026	15926	10471	27906	53	0	0	172
16	0	0	58449	29413	17364	50687	101	0	0	156
1	1	0	10912	5662	3284	9533	25	1	0	204
4	1	0	21195	11482	7061	19270	55	1	0	180
8	1	0	36012	18484	11405	31763	95	1	0	148
16	1	0	65629	33681	18869	56810	175	1	0	140
1	0	1	9590	4207	3045	8332	15	0	0	204
4	0	1	24994	10967	7614	21142	33	0	0	196
8	0	1	45489	19012	14109	38217	57	0	0	180
16	0	1	86521	35977	23584	69319	105	0	0	164
1	1	1	13876	6548	4359	12017	29	1	0	196
4	1	1	29669	13635	8983	25417	59	1	0	172
8	1	1	51954	22361	15940	43779	99	1	0	156
16	1	1	96567	42730	26741	79352	179	1	0	148

The maximum clock frequency results were obtained by double-registering input and output ports to reduce dependence on I/O placement. The inner level of registers used a separate clock signal to measure the path from the input registers to the first output register through the core. The results are post-implementation, using tool default settings except for high effort.

The resource usage results do not include the "characterization" registers and represent the true logic used by the core. LUT counts include SRL16s or SRL32s.

Clock frequency does not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification. The maximum achievable clock frequency and the resource counts might also be affected by other tool options, additional logic in the FPGA, using a different version of Xilinx tools, and other factors.

Port Descriptions

The SMPTE 2022-1/2 Video over IP Receiver core uses industry-standard control and data interfaces to connect to other system components. The following sections describe the various interfaces available with the core. Figure 2-1 provides an I/O diagram of the core. The number of TX_AXIS interfaces depends on the number of channels configured through the GUI. SEC_ETH_AXIS interface is available when seamless switching is enabled. M1_AXI interface is enabled when the FEC engine is included.

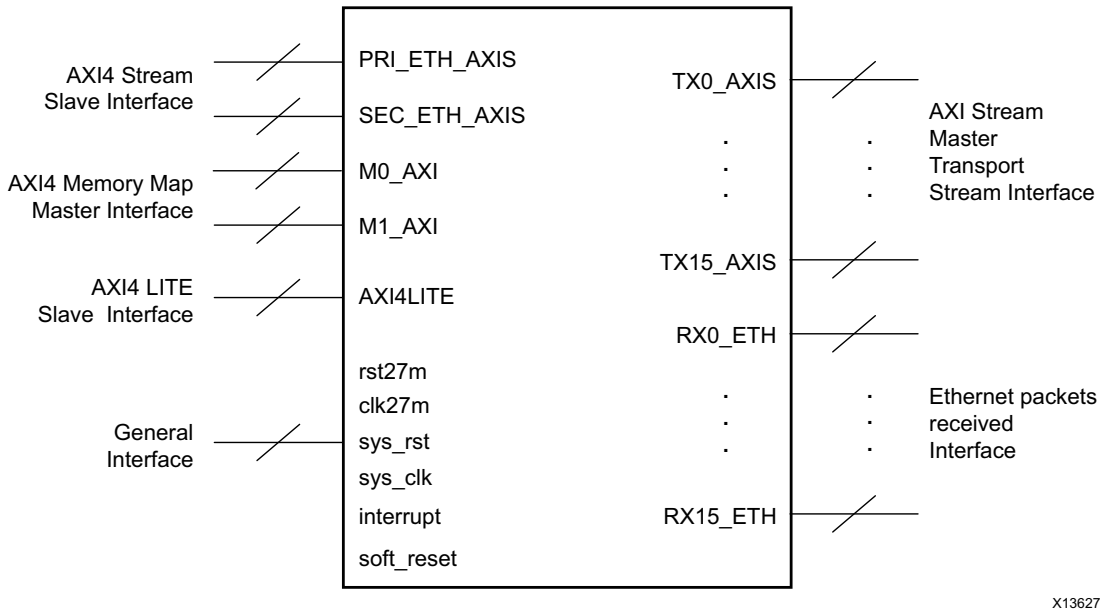

Figure 2-1: **SMPTE 2022-1/2 Video over IP Receiver Core Top Level Signaling Interface**

General Interface Signals

Table 2-5 summarizes the signals which are either shared by, or not part of, the AXI4-Stream, AXI-4, or AXI4-Lite control interfaces.

Table 2-5: **Common Interface Signals**

Signal Name	Direction	Width	Description
rst27m	In	1	27 MHz domain reset.
clk27m	In	1	27 MHz clock. Used for timekeeping.
sys_rst	In	1	System domain reset.
sys_clk	In	1	System clock.
Interrupt	Out	1	Interrupt from core.
Soft_reset	Out	1	Reset from core. From register bit.

AXI4 Memory Interface

The SMPTE 2022-1/2 Video over IP Receiver core uses an AXI4 interface to connect to the AXI4 interconnects. The AXI4 Interconnect provides access to external memory through the AXI DDR controller. See the *LogiCORE IP AXI Interconnect Product Guide* (PG059) [Ref 2] for more information.

Table 2-6: **AXI4 Memory Interface Signals**

Signal Name	Direction	Width	Description
m0_axi_awid	Out	1	Write Address Channel Transaction ID.
m0_axi_awaddr	Out	32	Write Address Channel Address.
m0_axi_awlen	Out	8	Write Address Channel Burst Length code.
m0_axi_awsize	Out	3	Write Address Channel Transfer Size code.
m0_axi_awburst	Out	2	Write Address Channel Burst Type.
m0_axi_awlock	Out	2	Write Address Channel Atomic Access Type.
m0_axi_awcache	Out	4	Write Address Channel Cache Characteristics.
m0_axi_awprot	Out	3	Write Address Channel Protection Bits.
m0_axi_awqos	Out	4	Write Address Channel Quality of Service.
m0_axi_awvalid	Out	1	Write Address Channel Valid.
m0_axi_awready	In	1	Write Address Channel Ready.
m0_axi_wdata	Out	128	Write Data Channel Data.
m0_axi_wstrb	Out	16	Write Data Channel Data Byte Strobes.
m0_axi_wlast	Out	1	Write Data Channel Last Data Beat.
m0_axi_wvalid	Out	1	Write Data Channel Valid.
m0_axi_wready	In	1	Write Data Channel Ready.
m0_axi_bid	In	1	Write Response Channel Transaction ID.
m0_axi_bresp	In	2	Write Response Channel Response Code.
m0_axi_bvalid	In	1	Write Response Channel Valid.
m0_axis_bready	Out	1	Write Response Channel Ready.
m0_axi_arid	Out	1	Read Address Channel Transaction ID.
m0_axi_araddr	Out	32	Read Address Channel Address
m0_axi_arlen	Out	8	Read Address Channel Burst Length code.
m0_axi_arsize	Out	3	Read Address Channel Transfer Size code.
m0_axi_arburst	Out	2	Read Address Channel Burst Type.

Table 2-6: **AXI4 Memory Interface Signals *(Cont'd)***

Signal Name	Direction	Width	Description
m0_axi_arlock	Out	2	Read Address Channel Atomic Access Type.
m0_axi_arcache	Out	4	Read Address Channel Cache Characteristics.
m0_axi_arprot	Out	3	Read Address Channel Protection Bits.
m0_axi_arqos	Out	4	AXI4 Read Address Channel Quality of Service.
m0_axi_arvalid	Out	1	Read Address Channel Valid.
m0_axi_arready	In	1	Read Address Channel Ready.
m0_axi_rid	In	1	Read Data Channel Data Transaction ID.
m0_axi_rdata	In	128	Read Data Channel Data.
m0_axi_rresp	In	2	Read Data Channel Response Code.
m0_axi_rlast	In	1	Read Data Channel Last Data Beat.
m0_axi_rvalid	In	1	Read Data Channel Valid.
m0_axi_rready	Out	1	Read Data Channel Ready.
m1_axi_awid	Out	1	Write Address Channel Transaction ID.
m1_axi_awaddr	Out	32	Write Address Channel Address.
m1_axi_awlen	Out	8	Write Address Channel Burst Length code.
m1_axi_awsize	Out	3	Write Address Channel Transfer Size code.
m1_axi_awburst	Out	2	Write Address Channel Burst Type .
m1_axi_awlock	Out	2	Write Address Channel Atomic Access Type.
m1_axi_awcache	Out	4	Write Address Channel Cache Characteristics.
m1_axi_awprot	Out	3	Write Address Channel Protection Bits.
m1_axi_awqos	Out	4	Write Address Channel Quality of Service.
m1_axi_awvalid	Out	1	Write Address Channel Valid.
m1_axi_awready	In	1	Write Address Channel Ready.
m1_axi_wdata	Out	128	Write Data Channel Data.
m1_axi_wstrb	Out	16	Write Data Channel Data Byte Strobes.
m1_axi_wlast	Out	1	Write Data Channel Last Data Beat.
m1_axi_wvalid	Out	1	Write Data Channel Valid.
m1_axi_wready	In	1	Write Data Channel Ready.
m1_axi_bid	In	1	Write Response Channel Transaction ID.

Table 2-6: **AXI4 Memory Interface Signals *(Cont'd)***

Signal Name	Direction	Width	Description
m1_axi_bresp	In	2	Write Response Channel Response Code.
m1_axi_bvalid	In	1	Write Response Channel Valid.
m1_axis_bready	Out	1	Write Response Channel Ready.
m1_axi_arid	Out	1	Read Address Channel Transaction ID.
m1_axi_araddr	Out	32	Read Address Channel Address
m1_axi_arlen	Out	8	Read Address Channel Burst Length code.
m1_axi_arsize	Out	3	Read Address Channel Transfer Size code.
m1_axi_arburst	Out	2	Read Address Channel Burst Type.
m1_axi_arlock	Out	2	Read Address Channel Atomic Access Type.
m1_axi_arcache	Out	4	Read Address Channel Cache Characteristics.
m1_axi_arprot	Out	3	Read Address Channel Protection Bits.
m1_axi_arqos	Out	4	AXI4 Read Address Channel Quality of Service.
m1_axi_arvalid	In	1	Read Address Channel Valid.
m1_axi_arready	In	1	Read Address Channel Ready.
m1_axi_rid	In	1	Read Data Channel Data Transaction ID.
m1_axi_rdata	In	128	Read Data Channel Data.
m1_axi_rresp	In	2	Read Data Channel Response Code.
m1_axi_rlast	In	1	Read Data Channel Last Data Beat.
m1_axi_rvalid	In	1	Read Data Channel Valid.
m1_axi_rready	Out	1	Read Data Channel Ready.

Ethernet AXI4 Stream Slave Interface

See the *LogiCORE Tri-Mode Ethernet MAC Product Guide* (PG051) [Ref 3] for more information.

Table 2-7: **AXI4 Stream Interface Signal**

Signal Name	Direction	Width	Description
pri_eth_rst	In	1	Active-high reset from TEMAC.
pri_eth_clk	In	1	Recovered clock from TEMAC.
pri_s_axis_tdata[7:0]	In	8	AXI4-Stream Data from TEMAC.

Table 2-7: **AXI4 Stream Interface Signal *(Cont'd)***

Signal Name	Direction	Width	Description
pri_s_axis_tvalid	In	1	AXI4-Stream Data Valid from TEMAC.
pri_s_axis_tlast	In	1	AXI4-Stream signal from TEMAC indicating an end of packet.
pri_s_axis_tuser	In	1	AXI4-Stream User Sideband Interface from TEMAC.
sec_eth_rst	In	1	Active-high reset from TEMAC.
sec_eth_clk	In	1	Recovered clock from TEMAC.
sec_s_axis_tdata[7:0]	In	8	AXI4-Stream Data from TEMAC.
sec_s_axis_tvalid	In	1	AXI4-Stream Data Valid from TEMAC.
sec_s_axis_tlast	In	1	AXI4-Stream signal from TEMAC indicating an end of packet.
sec_s_axis_tuser	In	1	AXI4-Stream User Sideband Interface from TEMAC.

AXI4-Lite Control Interface

The AXI4-Lite interface allows user to dynamically control parameters within the SMPTE 2022-1/2 Video over IP Receiver core. You can configure the core using an embedded ARM or soft system processor such as MicroBlaze.

You can control the core through the AXI4-Lite interface using read and write transactions to the SMPTE 2022-1/2 Video over IP Receiver register space.

The AXI4-Lite slave interface facilitates integrating the core into a processor system, or along with other video or AXI4-Lite compliant IP, connecting via the AXI4-Lite interface to an AXI4-Lite master. See the *LogiCORE IP AXI Interconnect Product Guide* (PG059) [Ref 2] for more information.

Table 2-8: **AXI4-Lite Interface Signals**

Signal Name	Direction	Width	Description
s_axi_clk	In	1	AXI4-Lite Clock.
s_axi_aresetn	In	1	AXI4-Lite Active-Low Reset.
s_axi_awaddr	In	9	AXI4-Lite Write Address Bus.
s_axi_awvalid	In	1	AXI4-Lite Write Address Channel Write Address Valid.
s_axi_wdata	In	32	AXI4-Lite Write Data Bus.
s_axi_wstrb	In	4	AXI4-Lite Write Data Channel Data Byte Strobes.
s_axi_wvalid	In	1	AXI4-Lite Write Data Channel Write Data Valid.

Table 2-8: **AXI4-Lite Interface Signals *(Cont'd)***

Signal Name	Direction	Width	Description
s_axi_awready	Out	1	AXI4-Lite Write Address Channel Write Address Ready. Indicates DMA ready to accept the write address.
s_axi_wready	Out	1	AXI4-Lite Write Data Channel Write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_bresp	Out	2	AXI4-Lite Write Response Channel. Indicates results of the write transfer.
s_axi_bvalid	Out	1	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid.
s_axi_bready	In	1	AXI4-Lite Write Response Channel Ready. Indicates target is ready to receive response.
s_axi_arvalid	In	1	AXI4-Lite Read Address Channel Read Address Valid
s_axi_arready	Out	1	Ready. Indicates DMA is ready to accept the read address.
s_axi_araddr	In	9	AXI4-Lite Read Address Bus
s_axi_rready	In	1	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_rdata	Out	32	AXI4-Lite Read Data Bus
s_axi_rresp	Out	2	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.
s_axi_rvalid	Out	1	AXI4-Lite Read Data Channel Read Data Valid.

AX4I-Stream Transport Interface.

Table 2-9: **Transport Stream AXI-Stream Interface Signals**

Signal Name	Direction	Width	Description
tx_axis_aresetn	Out	1	AXI4-Stream Active-Low reset.
tx_axis_aclk	In	1	AXI-4 Stream clock input.
tx_axis_tdata	Out	8	Transport stream Data out.
tx_axis_tvalid	Out	1	Transport stream Data Valid. A transfer takes place when both tx_axis_tvalid and tx_axis_tready are asserted.
tx_axis_tlast	Out	1	Indicates the boundary of a packet. Fixed at 0.
tx_axis_tuser	Out	1	User defined sideband information indicating synchronizing byte, 47h.
tx_axis_tready	In	1	Indicates that the slave can accept a transfer in the current cycle.

The transport stream data output behavior from the core transport stream interface is shown in Figure 2-2. Tx_axis_tuser is high when sending the synchronizing byte.

Tx_axis_tvalid is high when output data is valid. Tx_axis_tdata is updated when tx_axis_tready is high. Tx_axis_tlast is always low, and there is no idle byte.

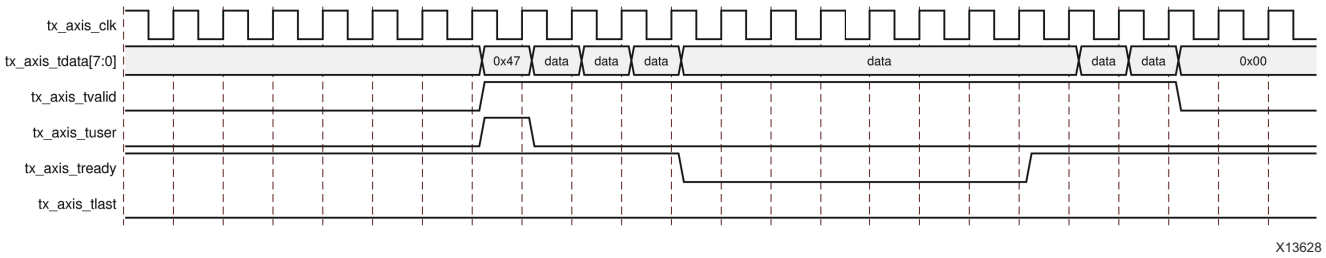

Figure 2-2: **SMPTE 2022-1/2 Video over IP Receiver Core Transport Stream AXI-Stream Interface**

Ethernet Packets Received Interface

Table 2-10: **Ethernet Packets Received Interface Signals**

Signal Name	Direction	Width	Description
rx_pri_rtp_pkt_recv	Out	1	Pulse indicating receiving of RTP packet from primary link. (Synchronous to pri_eth_clk)
rx_pri_rtp_seq_num	Out	16	Sequence number of RTP packet received from primary link. (Synchronous to pri_eth_clk)
rx_pri_rtp_ts	Out	32	Timestamp of the RTP packet received from primary link. (Synchronous to pri_eth_clk)
rx_sec_rtp_pkt_recv	Out	1	Pulse indicating receiving of RTP packets from secondary link. (Synchronous to sec_eth_clk)
rx_sec_rtp_seq_num	Out	16	Sequence number of RTP packet received from secondary link. (Synchronous to sec_eth_clk)
rx_sec_rtp_ts	Out	32	Timestamp of the RTP packet received from secondary link. (Synchronous to sec_eth_clk)
rx_rtp_pkt_buffered	Out	16	Amount of RTP packets buffered in the DDR for the channel. (Synchronous to sys_clk)
rx_rtp_pkt_transmit	Out	1	Pulse indicating consumption of RTP packet for TS output. (Synchronous to sys_clk)
rx_vid_lock	Out	1	Indication of channel locking to certain payload. (Synchronous to sys_clk)
rx_playout_ready	Out	1	Indication of channel ready for playing out the TS data. (Synchronous to sys_clk)

Register Space

The SMPTE 2022-1/2 Video over IP Receiver register space is partitioned into general and channel-specific registers.

Table 2-11: **AXI4-Lite Register Map**

Address (hex)	Register Name	Access Type	Default Value	Register Description
General Registers				
0x000	CONTROL	R/W	0	Bit 31-2: Reserved Bit 1: Register update Bit 0: Reserved
0x004	RESET	R/W	0	Bit 31-1: Reserved Bit 0: Soft reset
0x00C	CHANNEL_ACCESS	R/W	0	Bit 31: 0 - Primary, 1 - Secondary Bit 30-8: Reserved Bit 7-0: Channel to access
0x020	SYS_CFG	R	0	Bit 31: Seamless switching supported Bit 30: FEC recovery supported Bit 29-8: Reserved Bit 7-0: Number of channels supported
0x024	VERSION	R	0x01000000	Bit 31-24: Version major Bit 23-16: Version minor Bit 15-12: Version revision Bit 11-8: Patch ID Bit 7-0: Revision number
0x028	NETWORK_PATH_DIFFERENTIAL	R/W	0	Bit 31-9: Max delay between 2 streams in seamless switching, value based on 90kHz clock tick. Bit 8-1: Reserved Bit 0: 0 - disable seamless switching, 1- enable seamless switching
0x030	FEC_PROCESSING_DELAY	R/W	0	Bit 31-9: Delay on FEC packets before processing. Value is count based on 90kHz clock tick. Bit 8-0: Reserved
0x034	FEC_BASE_ADDR	R/W	0	Bit 31-0: Base address in the DDR to buffer the FEC packets
0x038	FEC_POOL_SIZE	R/W	0	Bit 31-0: Amount of Bytes in DDR to cater for the FEC buffer.
Channel-Specific Registers				

Table 2-11: **AXI4-Lite Register Map *(Cont'd)***

Address (hex)	Register Name	Access Type	Default Value	Register Description
0x080	IP_HDR_CFG	R/W	0	Bit 31-1: Reserved Bit 0: 0 – IPV4
0x084	IP_HDR_PARAM	R	0	Bit 31-16: Reserved Bit 15-8: Type of service (TOS) Bit 7-0: Time to live (TTL)
0x088	VLAN_TAG_INFO	R/W	0	Bit 31: 0 – without VLAN, 1- with VLAN Bit 30-16: Reserved Bit 15-0: VLAN tag
0x08C	DST_IP_ADDR	R/W	0	Bit 31-0: Destination IP address
0x09C	SRC_IP _ADDR	R/W	0	Bit 31-0: Source IP address
0x0AC	SRC_UDP_PORT	R/W	0	Bit 31-16: Reserved Bit 15-0: Source UDP port
0x0B0	DST_UDP_PORT	R/W	0	Bit 31-16: Reserved Bit 15-0: destination UDP port
0x0B4	MATCH_SEL	R/W	0	Bit 31-6: Reserved Bit 5: Match SSRC Bit 4: Match UDP dest port Bit 3: Match UDP src port Bit 2: Match Destination IP Bit 1: Match Source IP address Bit 0: Match VLAN tag
0x100	CHANNEL_ENABLE	R/W	0	Bit 31-1: Reserved Bit 0: 0 – disable, 1 – enable
0x110	SSRC	R/W	0	Bit 31-0: Synchronization Source
0x11C	PLAYOUT_DELAY	R/W	0	Bit 31-9: Wait time before TS data is played out on packet size lock, value based on 90kHz clock tick. Bit 8-0: Reserved
0x120	TS_STATUS	R	0	Bit 31-2: Reserved Bit 4-2: TS Packets per IP (1 to 7) Bit 1: transport stream packet size 0–188, 1–204 Bit 0: Packet size locked indicator
0x124	FEC_PARAM	R	0	Bit 31-22: Reserved Bit 21: FEC protect level: 1 - level B, 0 - level A Bit 20: FEC parameters locked Bit 19-10: Received D value Bit 9-0: Received L value

Table 2-11: **AXI4-Lite Register Map *(Cont'd)***

Address (hex)	Register Name	Access Type	Default Value	Register Description
0x12C	RTP_BASE_ADDR	R/W	0	Bit 31-0: Base address in the DDR to buffer the RTP packets
0x130	RTP_BUF_SIZE	R/W	0	Bit 31-16: Reserved Bit 15-0: Allocate the maximum number of RTP packets that can be stored in the DDR for the channel

CONTROL (0x000) Register

Bit 1 of the CONTROL register is a write-done semaphore for the host processor, which facilitates committing all user register updates in the channel space simultaneously. One set of registers (the processor registers) is directly accessed by the processor interface, while the other set (the active set) is actively used by the core. New values written to the processor registers are copied over to the active set if and only if the register update bit is set. Setting the bit to 0 before updating multiple registers and then setting the bit to 1 when updates are completed ensures all channel space registers are updated simultaneously.

RESET (0x004) Register

Bit 0 is software reset. When high, all the other registers and the core are held at reset state.

CHANNEL_ACCESS (0x00C) Register

Set the channel to access. All the primary link channels share the same set of register address in the channel space. For the secondary link channels, only 0x080 - 0x0B4 registers are available to set.

SYS_CFG (0x020) Register

Read-only current configuration of the core. Bit 31 high indicates seamless switching support. Bit 30 high indicates FEC engine is included. Bit 7-0 gives the number of channels available to use.

VERSION (0x03C) Register

Bit fields of the register facilitate software identification of the exact version of the hardware peripheral incorporated into a system. The core driver can take advantage of this read-only value to verify that the software is matched to the correct version of the hardware.

NETWORK_PATH_DIFFERENTIAL (0x028) Register

Set the maximum delay between primary and secondary link in seamless switching. The value is based on a 90kHz clock tick in Bit 31-9.

Bit 0 enables the seamless switching feature in the core. Setting it low blocks incoming Ethernet packets from the secondary link.

FEC_PROCESSING_DELAY (0x030) Register

Delay the incoming FEC packets before processing. The value is based on 90kHz clock tick in Bit 31-9.

FEC_BASE_ADDR (0x034) Register

This set the base address of the memory allocated in the DDR to store the FEC packets for recovery.

FEC_POOL_SIZE (0x038) Register

This register allocates the memory size in the DDR for FEC packets storage in bytes.

IP_HDR_CFG (0x080) Register

Set Bit 0 low for IPv4 support on the source and destination address.

IP_HDR_PARAM (0x084) Register

Read-only status on the IP header fields such Type of service (TOS) and Time to live (TTL).

VLAN_TAG_INFO (0x088) Register

Used in channel matching. Configure Bit 15-0 for VLAN tag matching. Set Bit 0 for valid VLAN tag.

DST_IP_ADDR (0x08C) Register

Used in channel matching. Configure Bit 31-0 for Destination IP address matching.

SRC_IP_ADDR (0x09C) Register

Used in channel matching. Configure Bit 31-0 for Source IP address matching.

SRC_UDP_PORT (0x0AC) Register

Used in channel matching. Configure Bit 15-0 for UDP Source Port matching.

DST_UDP_PORT (0x0B0) Register

Used in channel matching. Configure Bit 15-0 for UDP Destination Port matching.

MATCH_SEL (0x0B4) Register

This register helps to filter the incoming Ethernet packets according to the matching selection for the channel.

- Bit 5 matches RTP header SSRC field of the Ethernet packet to the configured SSRC (0x110) register.
- Bit 4 matches UDP header Destination Port field of the Ethernet packet to the configured DST_UDP_PORT (0x0B0) register.
- Bit 3 matches UDP header Source Port field of the Ethernet packet to the configured SRC_UDP_PORT (0x0AC) register.
- Bit 2 matches IP header Destination IP address field of the Ethernet packet to the configured DST_IP_ADDR (0x08C) register.
- Bit 1 matches IP header Source IP address field of the Ethernet packet to the configured SRC_IP_ADDR (0x09C) register.
- Bit 0 matches IEEE 802.1Q tag in the Ethernet frame to the configured VLAN_TAG_INFO (0x088) register.

CHANNEL_ENABLE (0x100) Register

Set Bit 0 to enable the channel operation.

SSRC (0x110) Register

Used in channel matching. Configure Bit 31-0 for RTP Synchronization Source identifier matching.

PLAYOUT_DELAY (0x11C) Register

Wait time before Transport Stream data is ready to play out upon packet size lock. The value based on a 90kHz clock tick in Bit 31-9.

TS_STATUS (0x120) Register

Read only status on the packet size locked by the channel.

When Bit 0 packet lock is high:

- Bit 4-2 shows the number of Transport Stream packets in an IP packet.
- Bit 1 shows the Transport Stream packet size. Bit 1 is low for 188 bytes and high for 204 bytes.

FEC_PARAM (0x124) Register

Read-only status on the FEC matrix size locked by the channel.

When Bit 20 FEC lock is high:

- Bit 9-0 contains the L value of FEC matrix.
- Bit 19-10 contains the D value of FEC matrix.
- Bit 21 indicates FEC protection level. Bit 21 is low for Level A stream and high for Level B.

RTP_BASE_ADDR (0x12C) Register

This register sets the base address of the memory allocated in the DDR to store the RTP packets for recovery and playout.

RTP_BUF_SIZE (0x130) Register

This register sets the maximum number of RTP packets that can be stored in the DDR for the channel. It has a limitation of 16 bits (Bit 15-0) and has to be in the value of (2^n–1).

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

The SMPTE 2022-1/2 Video over IP Receiver core is designed for broadcast applications that require bridging between the transport stream and 1 Gb/s Ethernet. The core accepts Ethernet packets encapsulated in accordance with SMPTE 2022-1/2 and extracts the transport stream packets. The packets are sent out via an AXI stream interface to multiple channels of ASI videos with DVB-ASI cores. The core receives Ethernet packets through an AXI4-Stream interface from 1 Gb/s Ethernet MAC. The core uses the AXI4 memory interface to transfer data between the core and external DDR memory. The register control interface is compliant with the AXI4-Lite interface.

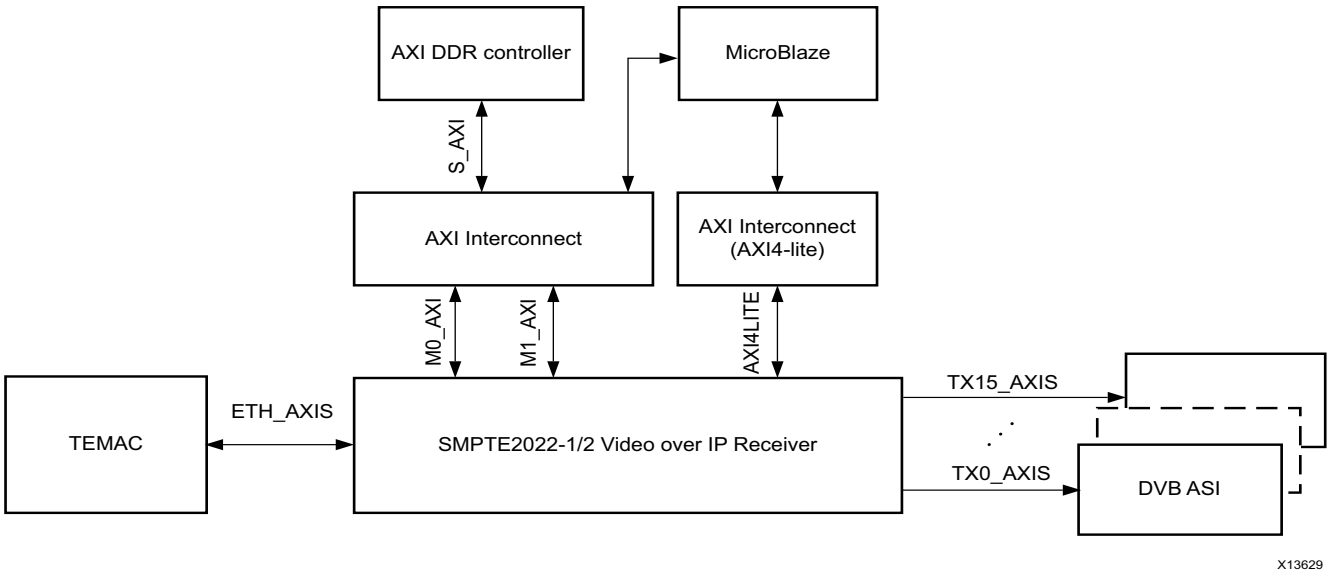

Figure 3-1: **SMPTE 2022-1/2 Video over IP Receiver System Built with Other Xilinx IP**

Note: In the SMPTE 2022-1/2 Video over IP Receiver core, you can include the FEC engine or enable seamless switching. FEC ensures the quality of compressed video by allowing the receiver to recover IP packets lost to network transmission errors. However, FEC increases the resource count in the device as well as the usage of external memory. Enabling seamless switching adds a redundancy

protection link for packets lost to network transmission errors, which also increases device resource count.

Clocking

The SMPTE 2022-1/2 Video over IP Receiver core has six main clock domains:

- Transport stream clock domain, tx_axis_aclk (recommended 148.5Mhz)
- System clock domain, sys_clk (refer to Fmax data)
- Primary link Ethernet clock domain, pri_eth_clk (125Mhz)
- Secondary link Ethernet clock domain, sec_eth_clk (125mhz)
- 27 MHz clock domain (clk27m)
- AXI4-Lite clock domain, s_axi_aclk (recommended 100Mhz)

Resets

The SMPTE 2022-1/2 Video over IP Receiver core has four main resets:

- Primary Ethernet link reset, pri_eth_rst
- Secondary Ethernet link reset, sec_eth_rst
- System domain reset, sys_rst
- 27Mhz domain reset, rst27m
- AXI4-Lite domain reset, s_axi_aresetn

The resets must be synchronous to their individual clock domains. A minimum of 16 clock cycles is recommended for the reset assertion. The pri_eth_rst and sec_eth_rst resets must be deasserted last.

Memory Requirements

The amount of DDR memory required by the SMPTE 2022-1/2 Video over IP Receiver core is determined by the number transport stream packets in an IP packet and the transport stream packet size for each channel.

Table 3-1 shows how to calculate the amount of DDR memory required by the core based on four instantiated transport stream channels and when FEC is included.

For an SMPTE 2022-2 packet containing 7 transport stream packets of 188 bytes, the core requires 1376 bytes in memory to store this RTP packet. If the number of RTP packets to buffer for each channel is set to 64, the memory utilization for each channel would be 88064 bytes.

The FEC packet buffer in memory is shared among all channels. For an FEC matrix size of 4x4, the core needs to store (4+4) x 2 = 16 FEC packets per channel. The core in this case minimally expects (4x4) x 2 = 32 RTP packets to be buffered in memory per channel for FEC recovery. The core requires 1408 bytes in the memory to store the accompanying SMPTE 2022-1 packet. The memory utilization for the FEC buffer is 90112 bytes.

Table 3-1: **Calculation of Memory Requirement for the SMPTE 2022-1/2 Video over IP Receiver**

Memory block	TS packets per IP	TS size	Required memory size per packet (bytes)	RTP_BUF_SIZE (0x130) Register	Memory utilization (bytes)	Base Address (HEX)
Channel 0	7	0	1376	63	88064	00000000
Channel 1	7	0	1376	63	88064	00015800
Channel 2	7	0	1376	63	88064	0002B000
Channel 3	7	0	1376	63	88064	00040800
FEC	7	0	1408	N.A.	90112	00056000

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP Integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 11] for detailed information.

Vivado Integrated Design Environment (IDE)

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click on the selected IP or select the Customize IP command from the toolbar or popup menu.

For details, see the sections, "Working with IP" and "Customizing IP for the Design" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the "Working with the Vivado IDE" section in the *Vivado Design Suite User Guide: Getting Started* (UG910).

Note: Figures in this chapter are illustrations of the Vivado IDE. This layout might vary from the current version.

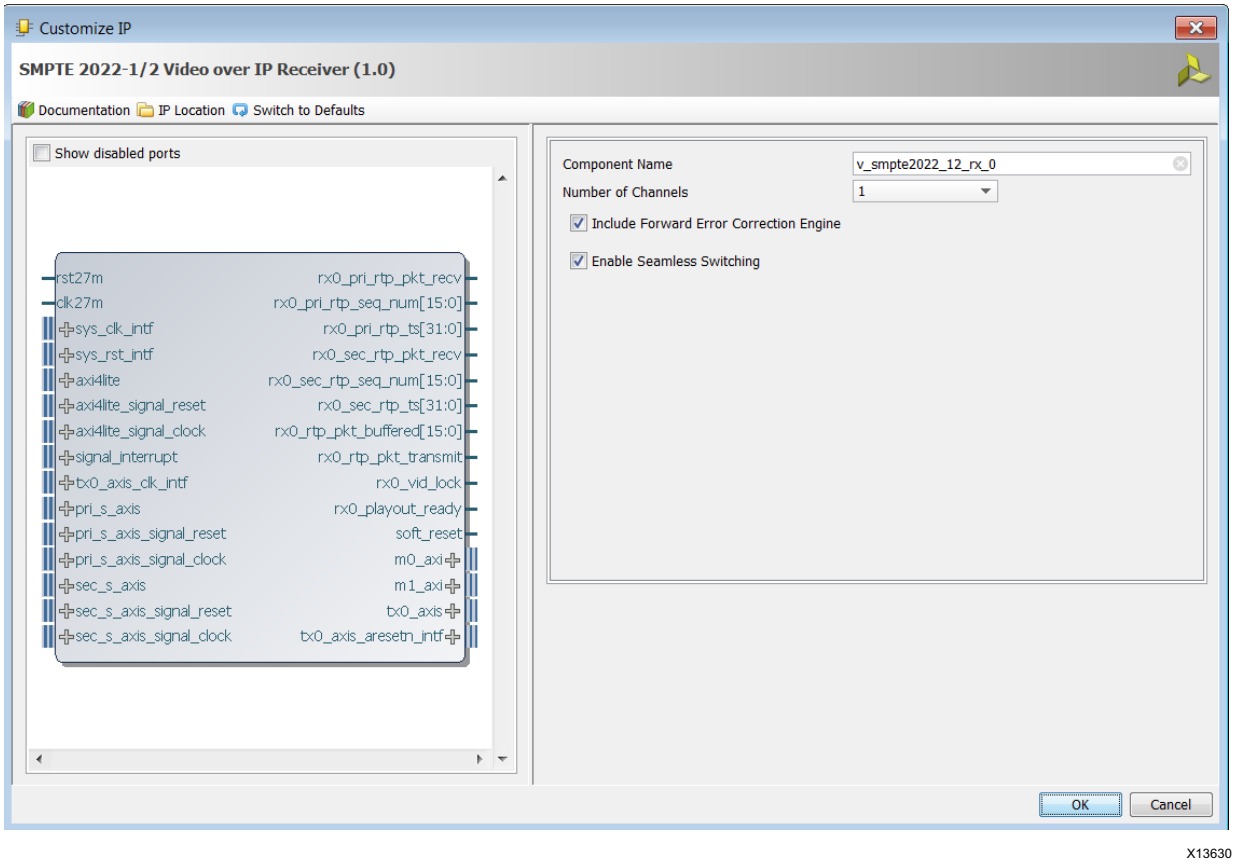

Figure 4-1: **SMPTE 2022-1/2 Video over IP Receiver Vivado Graphical User Interface**

The Vivado IDE displays a representation of the IP symbol on the left side and the parameter assignments on the right, as follows:

- **Component Name**: The base name of output files generated for the module. Names must begin with a letter and must be composed of characters a to z, 0 to 9 and "_". The name v_smpte2022_12_rx_v1_0 cannot be used as a component name.
- **Number of Channels**: Specifies the number of channels.
- **Include Forward Error Correction Engine**: When checked, the core is generated with FEC.
- **Enable Seamless Switching**: When checked, the core is generated with Secondary AXIS Ethernet Link to support hitless operation.

Output Generation

For details, see "Generating IP Output Products" in the *Vivado Design Suite User Guide: Designing with IP* (UG896). The Vivado design tools generate the files necessary to build the core and place those files in the <*project*>/<*project*>.srcs/sources_1/ip/<*core*> directory.

Constraining the Core

This chapter contains information about constraining the core in the Vivado® Design Suite environment.

Required Constraints

Constraints required for the core are clock frequency constraints for the clock domains described in Clocking in Chapter 3, Designing with the Core. Paths between the clock domains are constrained with a max_delay constraint and use the datapathonly flag, causing setup and hold checks to be ignored for signals that cross clock domains. These constraints are provided in the XDC constraints file included with the core.

Device, Package, and Speed Grade Selections

There are no device, package or speed grade requirements for this core. This core has not been characterized for use in low-power devices.

Clock Frequencies

See Maximum Frequencies in Chapter 2.

Clock Placement

There is no specific clock placement requirement for this core.

Banking

There is no specific banking rule for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Appendix A

Verification, Compliance, and Interoperability

The SMPTE 2022-1/2 Video over IP Receiver core has been validated using the Xilinx Kintex®-7 FPGA Broadcast Connectivity Kit.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

TIP: *If the IP generation halts with an error, there may be a license issue. See License Checkers in Chapter 1 for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the SMPTE 2022-1/2 Video over IP Receiver, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the SMPTE 2022-1/2 Video over IP Receiver. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record

AR: 54532

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Additional Resources.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Note: Access to WebCase is not available in all cases. Please login to the WebCase tool to see your specific support options.

Debug Tools

There are many tools available to address SMPTE 2022-1/2 Video over IP Receiver design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Tools

Vivado® lab tools insert logic analyzer and virtual I/O cores directly into your design. Vivado lab tools allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature represents the functionality in the Vivado IDE that is used for logic debugging and validation of a design running in Xilinx devices in hardware.

The Vivado lab tools logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Interface Debug

AXI4-Lite Interfaces

Read from a register that does not have all 0s as a default to verify that the interface is functional. Output `s_axi_aready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:

- The `s_axi_aclk and aclk` inputs are connected and toggling.
- The interface is not being held in reset, and `s_axi_areset` is an active-Low reset.
- The interface is enabled, and `s_axi_aclken` is active-High (if used).
- The main core clocks are toggling and that the enables are also asserted.
- If the simulation has been run, verify in simulation and/or a Vivado Lab tools capture that the waveform is correct for accessing the AXI4-Lite interface.

AXI4-Stream Interfaces

If data is not being transmitted or received, check the following conditions:

- If transmit <*interface_name*>_tready is stuck low following the <*interface_name*>_tvalid input being asserted, the core cannot send data.
- If the receive <*interface_name*>_tvalid is stuck low, the core is not receiving data.
- Check that the ACLK inputs are connected and toggling.
- Check that the AXI4-Stream waveforms are being followed.
- Check core configuration.
- Add appropriate core-specific checks

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

These documents provide supplemental material useful with this product guide:

1. *AXI Reference Guide* (UG761)
2. *LogiCORE IP AXI Interconnect Product Guide* (PG059)
3. *LogiCORE Tri-Mode Ethernet MAC Product Guide* (PG051)
4. *Vivado Design Suite User Guide - Logic Simulation* (UG900)
5. *Vivado Design Suite User Guide - Implementation* (UG904)
6. *Vivado Design Suite User Guide: Designing with IP* (UG896)
7. *ISE to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/02/2013	1.0	Initial Xilinx release.

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