LogiCORE IP Digital Pre-Distortion v4.0

XMP143 September 21, 2010 **Product Brief**

Introduction

Pre-distortion negates the non-linear effects of a power amplifier (PA) generated when transmitting a wide-band signal. Pre-distortion allows a PA to achieve greater efficiency by operating at higher output power while still maintaining spectral compliance, reducing system capital and operational expenditure.

The solution is targeted for basestations used in third and fourth generation (3G/4G) mobile technologies and beyond. It is a combination of hardware and embedded software processes that between them realize pre-distortion correction along with features that make for a fully engineered, practical, robust and self-contained solution. It is configurable both in feature selection and in usage to support a variety of clocking and resource requirements.

Features

- Algorithms
  - DPD correction with up to 33 dB of ACLR improvement
  - Pre-distortion correction architecture selection for cost-performance trade-off
  - Dynamics options
  - TDD support with automatic data selection
  - Quadrature modulator correction
  - PA saturation (overdrive) detection
  - Signal capture and analysis
- Physical Configuration Parameters
  - Selection of correction architectures of increasing performance/complexity
  - Selection of polynomial order of 5 or 7
  - Selection of one, two, four or eight transmit antennas
  - Clock to sample rate ratios from one to four
  - Optional quadrature modulation correction (QMC)
  - Optional hardware acceleration of coefficient estimation (HWA)
- Observation Signal Interface Options
  - Real IF feedback signal sampled at twice the pre-distortion sample rate with arbitrary IF frequency (optimal performance option)
  - Real IF feedback signal sampled at one times the pre-distortion sample rate with arbitrary IF frequency
  - Complex baseband feedback signal sampled at one times the pre-distortion sample rate
- Operational Modes and Debug
  - An easy-to-use software interface allows configuration, single-stepping and continuous automatic operation and gives access to signal measurements, data, diagnostic and status information.

Resource Requirements and Performance

Tables 1, 2 and 3 show the resource utilisation for selected physical configuration parameters for the supported device families. Correction architecture D generally gives the highest performance.

Table 1: **Resource Utilization on Virtex-5 (5vlx155-ff1153-1 on ISE 12.3)**

Number of Transmit Paths	Architec-ture	Clocks/ Sample	QMC	HWA	FFs	LUTs	Slices	Block RAMs 36K[1]	DSP48Es
1	D	4	False	False	3340	2979	1550	55	14
1	D	4	False	True	5138	4117	2045	69	34
1	D	4	True	False	3449	2957	1435	55	17
1	D	4	True	True	5253	4101	2204	71	37
2	D	4	False	False	4348	3758	2045	63	21
4	D	4	False	False	6355	5123	2796	83	35
8	D	4	False	False	10391	7913	4080	115	63

Notes:

1. For Virtex-5 the BRAM usage is reported as a number of 36K BRAMs. Typically 2x18K BRAMs are combined and reported as 36K.

Table 2: **Resource Utilization on Virtex-6 (6vsx315t-ff1759-1 on ISE 12.3)**

Number of Transmit Paths	Architec-ture	Clocks/ Sample	QMC	HWA	FFs	LUTs	Slices	Block RAM 36K/18K[1]	DSP48E1s
1	D	4	False	False	3142	2956	1188	55/0	14
1	D	4	False	True	4903	4262	1802	64/10	34
1	D	4	True	False	3206	2948	1282	55/0	17
1	D	4	True	True	5009	4299	1740	64/10	37
2	D	4	False	False	4131	3600	1680	63/0	21
4	D	4	False	False	6101	5050	2101	83/0	35
8	D	4	False	False	10073	8091	3322	115/0	63

Notes:

1. In some configurations Virtex-6 uses a number of 18K BRAMs in addition to full 36K BRAMs.

Table 3: **Resource Utilization on Spartan-6 (6slx150-fgg900-2 on ISE 12.3)**

Number of Transmit Paths	Architec-ture	Clocks/ Sample	QMC	HWA	FFs	LUTs	Slices	Block RAMs 18K/9K[1]	DSP48Es
1	D	2	False	False	3694	3362	1591	105/3	19
1	D	2	False	True	5497	4559	1891	128/5	39
1	D	2	True	False	3775	3323	1585	105/3	22
1	D	2	True	True	5612	4547	1991	128/5	42
2	D	2	False	False	5219	4355	1951	121/3	30
4	D	2	False	False	8255	6414	2788	161/3	52

Notes:

1. Spartan-6 cases use a number of 9K BRAMS in addition to full 18K BRAMs.

Power Amplifer Correction Performance Example

The core has been tested with signals representative of various air interface standards. Testing is carried out with an industry standard radio card and power amplifier. Figure 1 shows the performance for a WCDMA test case with different correction architectures.

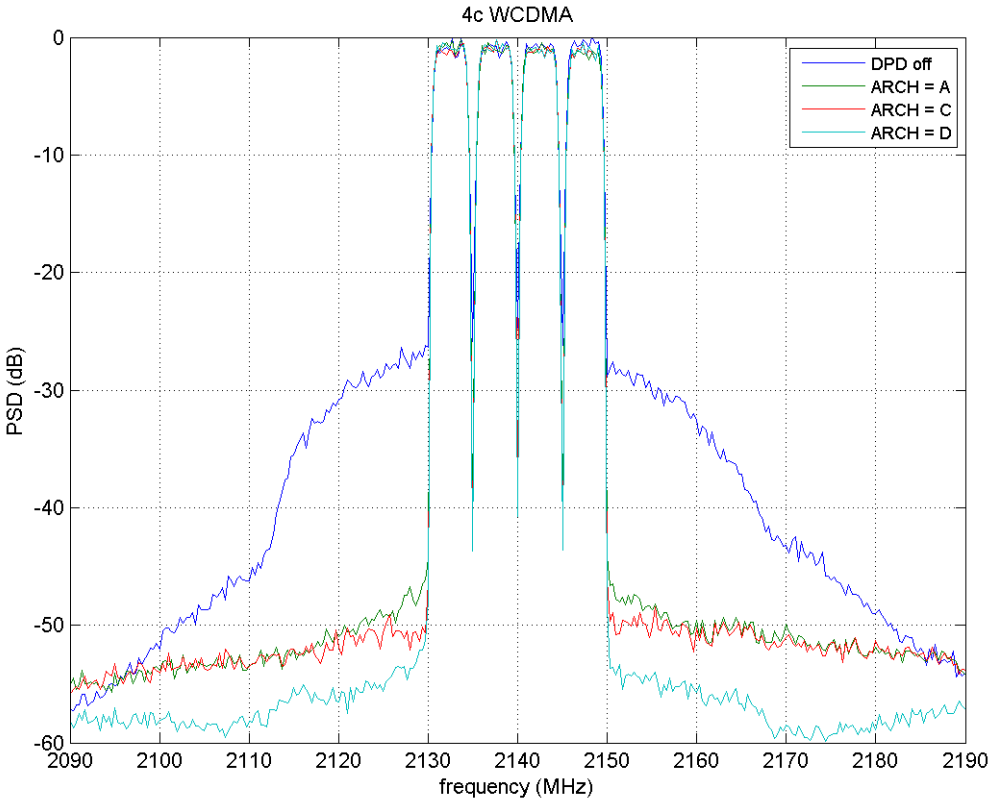

Figure 1: **Spectra for Four WCDMA Carriers before and after DPD**

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to each core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for each core. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator software v12.3 and later. The Xilinx CORE Generator system is shipped with Xilinx ISE Design Suite development software.

To order Xilinx software, contact your local Xilinx sales representative.

Information on additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/21/10	1.0	Product release 12.3

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