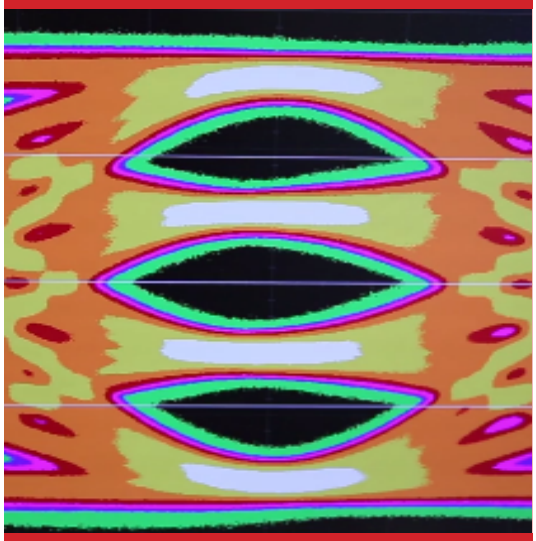


Programmable System Integration
- Up to 3.6M system logic cells
- Up to 500Mb of total on-chip memory for integration
- Integrated 100G Ethernet MAC with RS-FEC and 150G Interlaken cores
- PCI Express® Gen 3x16

Increased System Performance
- Up to 48 PAM4 transceivers operating at 58Gb/s deliver multi-terabit systems
- 32 transceivers operating at 32.75Gb/s provide 25G interoperability
- 38 TOP/s DSP compute performance
- 2,666Mb/s DDR4 in the mid-speed grade

BOM Cost Reduction
- Eliminates discrete gearbox ICs
- VCXO and fractional PLL integration reduces clocking component cost

Total Power Reduction
- Up to 50% lower system power vs. a 28G discrete gearbox solution
- Voltage scaling options for performance and power
- Tighter CLB packing reduces dynamic power

XILINX
ALL PROGRAMMABLE™

Virtex UltraScale+ 58G PAM4 Transceiver-Enabled FPGA: Fastest Transceiver in a Programmable Device

Virtex® UltraScale+™ 58G-enabled devices enable superior performance-per-watt, form factor, as well as system-level cost for implementing 100G/400G data center interconnect lanes. The integrated 58G PAM4 transceiver technology doubles the transmission rate on existing platforms, providing seamless migration of existing systems to next-gen backplane, optics, and high-performance interconnects. These devices include 25% more 100G Ethernet MAC integrated blocks and on-chip KP4-FEC (forward error correction) integrated blocks to reduce solution complexity and costs for tomorrow's most demanding 50G, 100G, 200G, and 400G interconnects.

Enabling Machine Learning in the Data Center and at the Edge

Virtex UltraScale+ 58G devices enable the smart deployment of reconfigurable custom workloads such as machine learning, database acceleration, video transcoding, and security or network acceleration offload, implemented either at the core or at the edge, on a single device with no need for external gearbox ICs.

Building on the Success of Xilinx's UltraScale Portfolio

The UltraScale+ family of FPGAs, 3D ICs, and MPSoCs combines new memory, 3D-on-3D, and MPSoC technologies, delivering a generation ahead of value. To enable an even higher level of performance and integration, the UltraScale+ family also includes a new IP interconnect optimization technology, SmartConnect. Built upon Xilinx's UltraScale™ architecture, these devices leverage a significant boost in performance-per-watt using 16FF+ FinFET 3D transistors from the #1 service foundry in the world, TSMC. Xilinx provides scalability and package migration for the lowest risk and the highest value programmable technology.

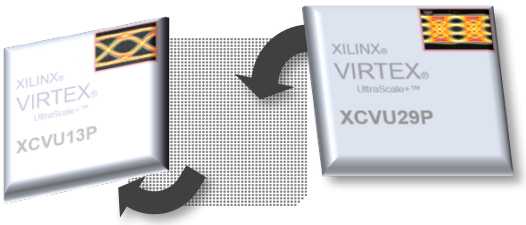
FEATURES OVERVIEW

16nm low power FinFET+ process technology from TSMC Industry leading process from the #1 service foundry delivers a step function increase in performance-per-watt	• The same scalable architecture and tools from Virtex UltraScale FPGAs
Massive I/O bandwidth and dramatic latency reduction 58G transceivers allow full 50GE lanes without the use of discrete gearboxes	• 28G and 58G backplane support • 32.75G and 58G chip-to-chip and chip-to-optics support • High-Density I/O for smaller area and greater power efficiency per pin
Integrated 100G Ethernet MAC and 150G Interlaken cores ASIC-class cores for breakthrough performance in packet processing	• 60K–100K system logic cell savings per port • Up to 90% dynamic power savings vs. soft implementation • Built-in KP4-FEC for PAM4 optics and backplanes • Built-in KR4-FEC (Ethernet MAC) for optics error correction
UltraRAM for deep memory buffering Up to 432Mb for SRAM device integration	• For deep packet and video buffering • 8X capacity-per-block vs. traditional embedded memory • Deep-sleep power modes
Enhanced DSP slices for diverse applications Enabling a massive jump in fixed-and floating-point performance	• Up to 38 TOP/s of INT8 DSP computation • Double-precision floating point using 30% fewer resources • Complex fixed-point arithmetic in half the resources
Massive memory interface bandwidth Next-generation DDR and serial memory support	• DDR4 support of up to 2,666 Mb/s • Support for server-class DIMMs • Hybrid Memory Cube serial memory support of up to 30G
SmartConnect Technology System-wide interconnect optimization tools and IP	• Matches optimal AXI interconnect to the design • Automatic interface bridging • Additional 20–30% advantage in performance-per-watt
Next-generation routing, ASIC-like clocking, and enhanced CLB Enabling breakthrough speeds with high utilization	• Lower skew, faster performing clock networks • Up to one speed-grade advantage vs. comparable solutions • Efficient CLB use & placement for reduced interconnect delay
Integrated blocks for PCI Express Complete end-to-end solution for multi-100G ports	• Gen3 x16 for 100G bandwidth per block • Expanded virtualization for data center applications • Enhanced tag management for increased buffer space
High-speed memory cascading Removes key bottlenecks in DSP and packet processing	• Eliminates logic usage when building deep memories • Reduces routing congestion • Lowers dynamic power consumption
Next-generation security Enhanced features to protect IP and prevent tampering	• AES-GCM decryption, RSA-2048 authentication • DPA countermeasures and permanent tamper penalty • Robust SEU performance

Take the NEXT STEP

Start by contacting your Xilinx Sales Representative today:

- Arrange an on-premises transceiver performance evaluation
- Learn how you can start designing for Virtex UltraScale+ 58G-Enabled FPGAs using the VU13P in production NOW



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