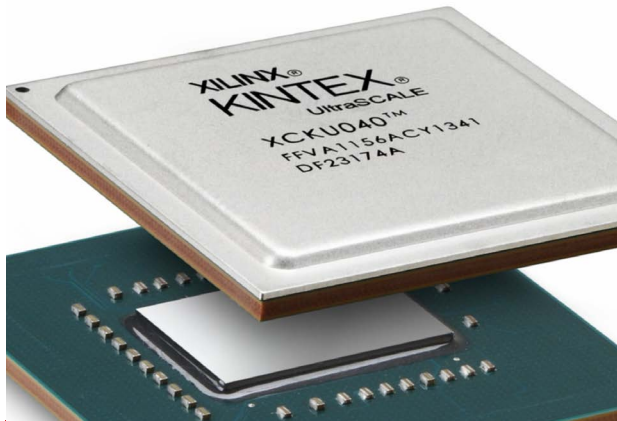


Kintex UltraScale FPGA



Programmable System Integration

- Up to 1.5M system logic cells
- Integrated 100G Ethernet MAC and 150G Interlaken cores
- Integrated blocks for PCI Express®

Increased System Performance

- 30G transceivers for chip-to-chip, chip-to-optics, 28G backplanes
- 2,400Mb/s DDR4 for robust operation over varying PVT

BOM Cost Reduction

- 12.5Gb/s transceivers in slowest speed grade
- VCXO integration reduces clocking component cost

Total Power Reduction

- Up to 40% lower power vs. Kintex-7 FPGAs
- Key process and architectural innovations such as ASIC-like clocking and block RAM cascading
- Range of device power options and design tool optimization methods, including optimal logic packing and power optimization

Expanding Price-Performance-Per-Watt for the Mid-range

Kintex® UltraScale™ devices deliver ASIC-class system-level performance, clock management, and power management for next-generation price-performance-per-watt. These second generation devices expand the mid-range by delivering increased throughput with reduced latency for medium-to-high volume applications, including 100G networking, wireless infrastructure, and other DSP-intensive applications. Based on the ASIC-class advantage of the Xilinx UltraScale architecture, Kintex UltraScale devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

Re-architecting the core for massive bandwidth with the UltraScale architecture

The UltraScale families are based on the first All Programmable architecture to span multiple nodes from planar through FinFET technologies and beyond, while also scaling from monolithic through 3D ICs. The UltraScale architecture provides diverse benefits and advantages to an array of markets and applications. The architecture combines enhancements in the configurable logic block (CLB), a dramatic increase in device routing, and a revolutionary ASIC-like clocking architecture with high-performance DSP, memory interface PHYs, and serial transceivers. All UltraScale architecture-based FPGAs are capable of pushing the system performance-per-watt envelope, enabling breakthrough speeds, at high utilization. High system performance and multiple power reduction innovations make the UltraScale architecture the logical choice for many next-generation applications.

Building on the success of Xilinx's innovations with 7 series

Built with TSMC's 20nm SoC technology, the Kintex UltraScale family of FPGAs combine the industry's best transceivers, integrated PCI Express, 100G Ethernet MAC/PCS, Interlaken blocks, analytical placement and co-optimization, and careful process optimization to achieve the highest performance-per-watt attainable at the process node. In addition, the Kintex UltraScale family leverages new IP Integrator technology, which allows designers to quickly stitch IP together by designing at the interface level. The IP Integrator provides correct-by-construction signal-level connectivity to enable an even higher level of productivity and integration.

FEATURES OVERVIEW
20nm SoC process technology from TSMC

Industry-leading process from the #1 service foundry delivers a step function increase in performance-per-watt

- 40% greater performance-per-watt over Kintex-7 FPGAs

Next-generation routing, ASIC-like clocking & enhanced fabric

Enabling breakthrough speeds at over 90% utilization

- Smaller area and greater power consistency
- Efficient CLB use and placement for reduced interconnect delay

Enhanced DSP slices for diverse applications

Enabling a massive increase in fixed- and floating-point performance

- Up to 8.2TeraMACs of bandwidth at 741MHz operation
- Double-precision floating point in 30% fewer resources
- Complex fixed-point arithmetic in half the resources

Integrated 100G Ethernet MAC and 150G Interlaken cores

ASIC-class cores for breakthrough performance in packet processing

- 60K–100K system logic cell savings per port
- Up to 80% dynamic power savings vs. soft implementation

Massive memory interface bandwidth

High-performance DDR and serial memory support

- DDR4 support of up to 2,400Mb/s
- Support for server-class DIMMs – 8X capacity vs. Kintex-7 FPGAs
- Hybrid Memory Cube serial memory support of up to 15G

Massive I/O bandwidth and dramatic latency reduction

2.5X greater serial bandwidth than Kintex-7 FPGAs

- Eliminates fabric usage when building deep memories
- Reduces routing congestion
- Reduces dynamic power consumption

High-speed memory cascading

Removes key bottlenecks in DSP and packet processing

- DDR4 support of up to 2,400Mb/s
- Support for server-class DIMMs – 8X capacity vs. Virtex-7 FPGAs
- Hybrid Memory Cube serial memory support of up to 30G

Integrated blocks for PCI Express

Complete end-to-end solution for multi-50G ports

- Gen3 x8 for 50G bandwidth per block
- Single-root I/O virtualization for data center applications
- Tandem field update for maximum system flexibility

Up to 40% power savings over Kintex-7 FPGAs

Total power reduction at every level: static, dynamic, I/O, and transceiver

- FPGA-optimized process and operating point
- Power-optimized transceivers and block RAM
- Fine-grained clock gating and superior logic utilization

Next-generation security

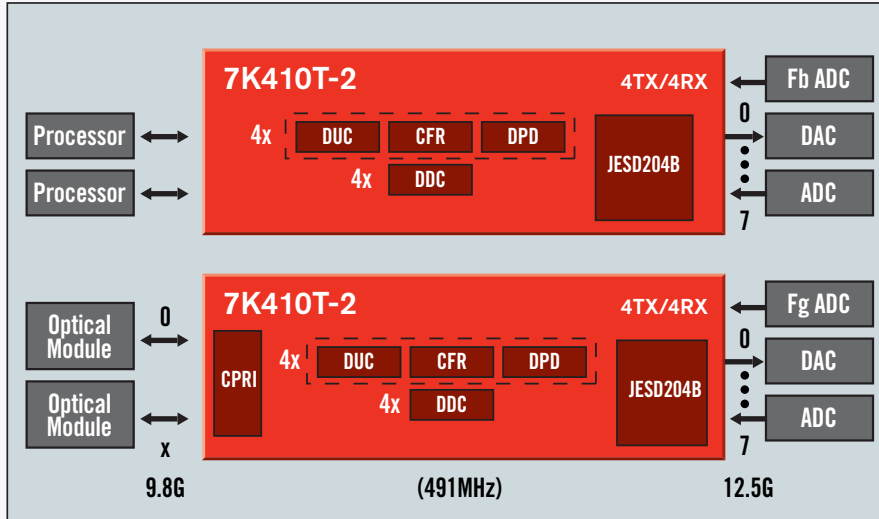
Enhanced features to protect IP and prevent tampering

- AES-GCM decryption, RSA-2048 authentication
- DPA countermeasures and permanent tamper penalty

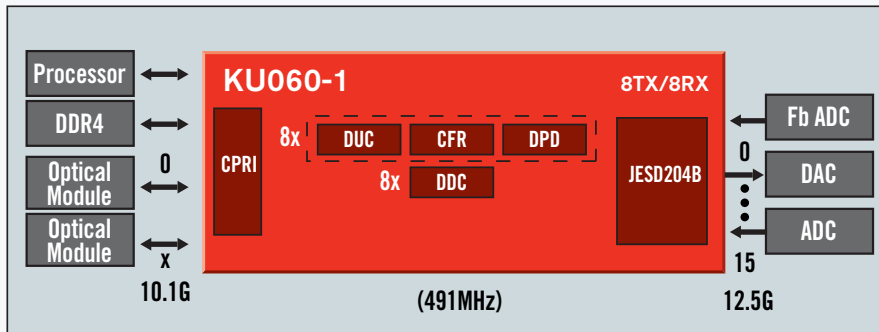
DFE 8x8 100MHz TD-LTE Radio Unit

Key UltraScale Portfolio Benefits:

Existing Infrastructure



Kintex UltraScale Solution



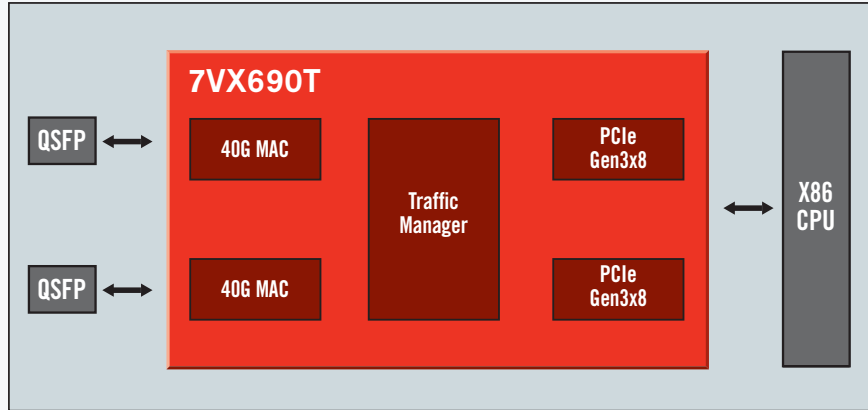
Solution Benefits
System Integration 2 Device ⇌ 1 Device
System Performance +25%
BOM Cost -40%
Total Power -31%
Accerated Productivity Vivado HLS Radio & Connectivity IP

- 8x8 multi-standard radio platform in a single, low power device. One platform for multiple regions, antenna configurations and standards for fast, cost effective deployment
- UltraScale FPGA fabric for 491MHz performance in slowest speed grade device allows for compact, high performance implementation
- JESD204B in all available speed grades to reduce power and operating expenses
- Higher device utilization to permit implementation in smaller, lower power devices
- Tightly integrated development tool flow using OpenCL, Vivado High-Level Synthesis, and IP Integrator for fast algorithm development
- SmartCORE™ IP DPD, CFR, Filter IP, specialized ecosystem IP for reduced time to integration

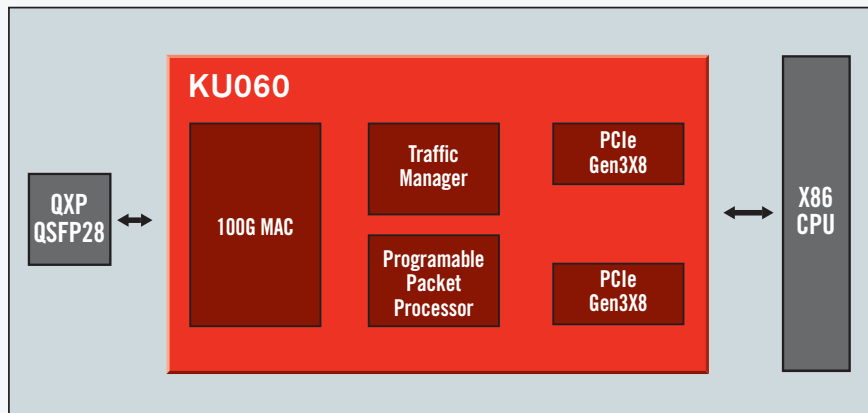
100G NIC with PP Integration

Key UltraScale+ Portfolio Benefits:

Existing Infrastructure



Kintex UltraScale Solution



Solution Benefits
System Integration 1 Device ⇔ 1 Device
System Performance +20%
BOM Cost -71%
Total Power -30%
Accelerated Productivity Integrated 100G Ethernet MAC Integrated PCIe Gen3

- Integration of single CXP module for higher front panel density, doubling front panel optics capacity, leading to doubling bandwidth on a line card
- Reduce system latency and power through granular clock gating and off-loading CPU functions
- Integrated 100G Ethernet and PCI Express Gen3 cores provide lowest latency implementation while retaining benefits of programmability
- Accelerated design productivity by leveraging OpenCV, Vivado High-Level Synthesis, and IP Integrator in a tightly integrated tool flow
- Reduced time to integration with SmartCORE IP, specialized ecosystem IP and software, and operating systems

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