

16.1 A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC

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In recent years, the need for high performance RF sampling ADCs has driven impressive developments of pipelined-SAR and pipelined ADCs, all supported by time-interleaving [1-4]. All these designs use a closed loop MDAC amplifier in the first stage and digital calibration/equalization to alleviate finite gain, settling and memory effects, but the closed-loop amplifier remains a scaling bottleneck. In this work, a three-stage asynchronous pipelined-SAR with open-loop integrator-based amplifiers is used to maximize the sampling frequency, resolution and linearity. The solution is mostly supported by dynamic circuits and multiple calibration loops to reduce cost, power and noise, maximize process portability and support production testability.

Figure 16.1.1a illustrates the architecture of the ADC. The design is configurable for dual-channel conversion (In0 and In2) at 2GS/s or single-channel conversion (In1) at 4GS/s. This provides flexibility to support IQ and direct RF communication architectures, respectively. Only two of four input buffers (IB) are enabled in each configuration. Each 2GS/s ADC unit consists of four interleaved 500MS/s sub-ADC slices and a sampling network composed of a front-end switch and four channel switches used to interleave the four ADC slices without time-skew calibration requirements. In IQ mode, only offset and gain mismatch calibration is required. In RF mode, the clock is divided by 2 and sent to each 2GS/s unit ADC out of phase. In this case, an additional digitally controllable delay cell is used to minimize the sampling time-skew between 2GS/s units. Finally, each 500MS/s sub-ADC slice is supported by foreground (FG) and background (BG) calibration loops.

Figure 16.1.1b shows the topology of each sub-ADC. It uses three asynchronous 5b SAR stages separated by two residue amplifiers (RA). For speed reasons, each stage uses a split-capacitor MDAC to maintain constant common mode and five cascaded dynamic comparators. The use of two RAs reduces the noise/offset requirements of the back-end comparators. This allows aggressive optimization of comparator decision time and use of a single comparator design across the pipeline chain. A single RA design is used to reduce design/verification effort, with only a minor penalty to power consumption. The gain of the integrating RA is adjusted by appropriately sizing its load capacitance. The FG calibration corrects comparator offsets, RA offset and gain and capacitor mismatch. The BG calibration adjusts the RA gain and comparator offset drift due to temperature and voltage variations during operation. FG and BG calibrations follow the approach used in [5].

Figure 16.1.2a details the clock interface of the pipelined-SAR ADC. The integration time of the RAs varies considerably across PVT, and leakage limits the achievable performance of the ADC at low sampling frequencies if using a synchronous clocking scheme. So, an asynchronous clocking scheme is selected to maintain best performance across the sampling frequency range. By using integrating RAs, it is necessary to completely reset the sampling capacitors of stage 2 and stage 3 before connecting them to the preceding RA. A modular handshaking scheme is used to guarantee that the RA waits for the next stage to be ready before starting integration. The block diagram is shown in Fig. 16.1.2b and the sequence of events in Fig. 16.1.2c. This functionality is used by all stages.

Figure 16.1.3a shows the topology of the IB. It consists on an NMOS source follower with current feedback. The feedback loop maximizes the linearity of the source follower by using the fact that any signal-dependent increase in current drawn by A2 decreases the current flowing into the source of A3. This decrease is then fed back through the current mirror A4-A7. A current ratio of 1:4 between A7 and A5 is used to optimize noise and speed. Parasitic capacitance in this loop needs to be minimized to reduce the amount of AC current lost to charging parasitic capacitors.

Figure 16.1.3b shows the topology of the RA. While an open-loop integrator-type amplifier avoids the challenges associated with stability and settling, it does have stringent linearity requirements. A folded-cascade OTA is used to minimize the supply voltage. A linearized input differential pair [6] is selected because the first-stage quantizes only 5b and the residue is too large for the required linearity using a simple differential pair. Switches are used to disable the RA when not in use. Bias voltages are kept stable to allow fast start-up and a maximum of 350ps integration time for both RAs. A switched-capacitor common mode feedback is used to set the output common mode. Figure 16.1.3c illustrates the integration time generation used to calibrate the gain of the amplifier. It consists of two current-starved inverters. Programmable capacitive loads are used to support 1ps steps.

The ADC is manufactured in 16nm CMOS. The total area including digital circuitry and supply decoupling is 1.04mm². Figure 16.1.7 presents the die micrograph. Figure 16.1.4 shows INL and DNL within +/-1.5LSB and +/-0.3LSB respectively, measured at 4GS/s in RF mode. Figure 16.1.4 also shows the capacitance and comparator calibration codes for thousands of samples demonstrating some of the self-test features of the design used for efficient production testing and debug. Figure 16.1.5 (top-left) presents the output spectra with -1dBFS, 1.9GHz input signal at 4GS/s in RF mode. SFDR and SNDR are 67.0dB and 57.3dB. The distortion is dominated by HD2/HD3 and all remaining spurs are lower than -80dBFS. Figure 16.1.5 (bottom) shows the SFDR and SNDR vs. input frequency (left) and vs. sampling frequency (right). In RF mode, the peak SFDR and SNDR are 76dB and 64dB respectively at 200MHz and 61dB and 55dB respectively at 2.3GHz input frequency. This level of performance is maintained up to 4.8GS/s. Performance measurements for IQ mode are also illustrated for completeness. Figure 16.1.5 (top-right) shows power dissipation vs. sampling frequency. The RF ADC consumes 513mW at 4GS/s, including 282mW dissipated by the input buffers, 142mW consumed by the ADC cores and 89mW dissipated by the digital calibration blocks.

Figure 16.1.6 summarizes the relevant specs and compares this ADC to several recently published ADCs. This work shows the best peak SNDR. At Nyquist, this ADC achieves a Walden FOM of 214.2fJ/conv-step and a Schreier FOM of 153.2dB which compares well to existing designs and clearly shows that the chosen architecture is a viable alternative to conventional closed loop pipeline solutions.

References:

- [1] J. Wu, et al., "A 4GS/s 13b Pipelined ADC with Capacitor and Amplifier Sharing in 16nm CMOS," *ISSCC*, pp. 466-467, Feb. 2016.
- [2] M. Straayer, et al., "A 4GS/s Time-Interleaved RF ADC in 65nm CMOS with 4GHz Input Bandwidth," *ISSCC*, pp. 464-465, Feb. 2016.
- [3] A. Ali, et al., "A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither," *IEEE Symp. VLSI Circuits*, pp. 206-207, June 2016.
- [4] M. Brandolini, et al., "A 5GS/s 150mW 10b SHA-Less Pipelined/SAR Hybrid ADC in 28nm CMOS," *ISSCC*, pp. 468-469, Feb. 2015.
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- [6] A. Demosthenous, et al., "Low-Voltage MOS Linear Transconductor/Squarer and Four-Quadrant Multiplier for Analog VLSI," *IEEE TCAS-I*, vol. 52, no. 9, pp. 1721-1731, Sept. 2005.

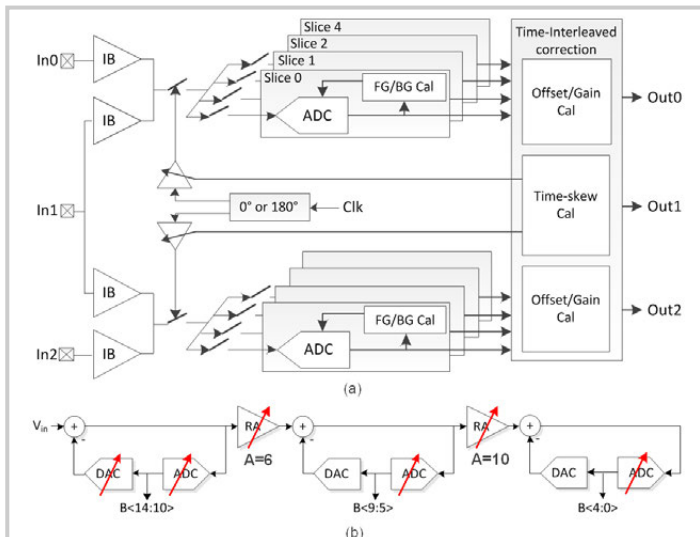


Figure 16.1.1: Block diagrams: (a) time-interleaved ADC; (b) three-stage asynchronous pipelined-SAR.

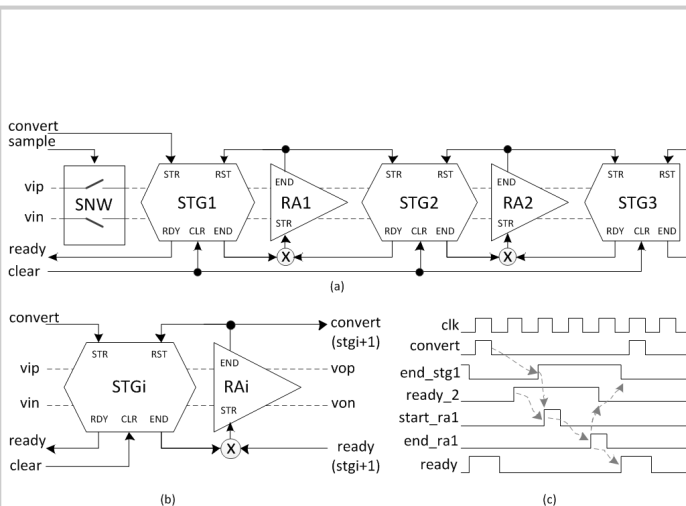


Figure 16.1.2: (a) Clock interface (b) Inter-stage block diagram (c) Inter-stage timing diagram.

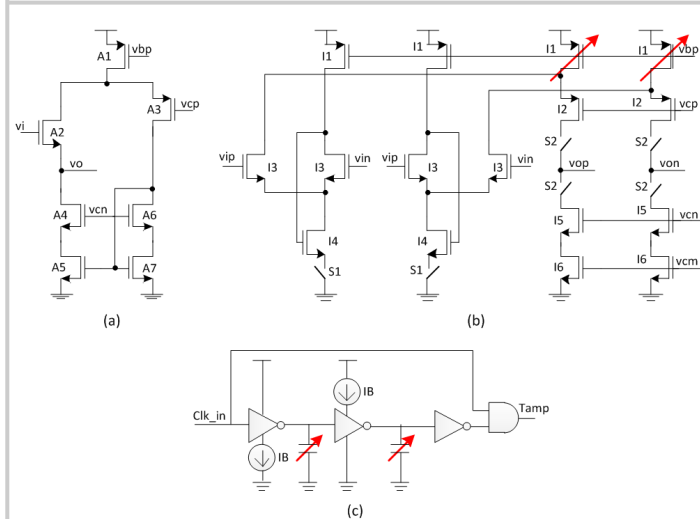


Figure 16.1.3: (a) Input buffer (b) residue amplifier (c) integration time calibration.

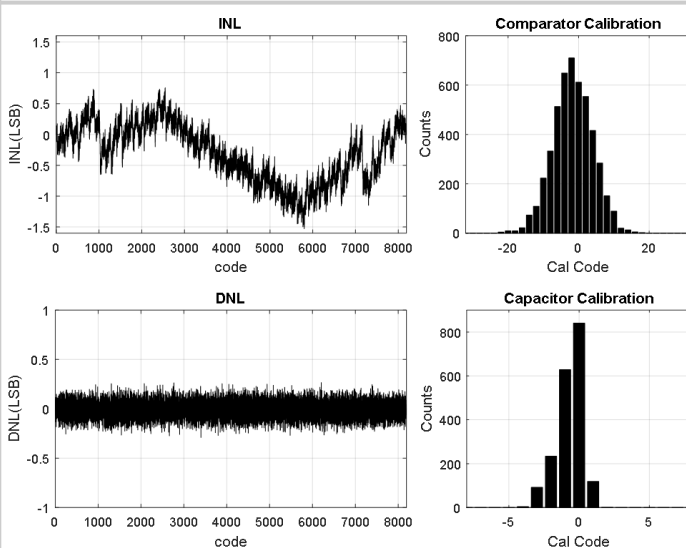


Figure 16.1.4: INL/DNL performance and calibration code histograms.

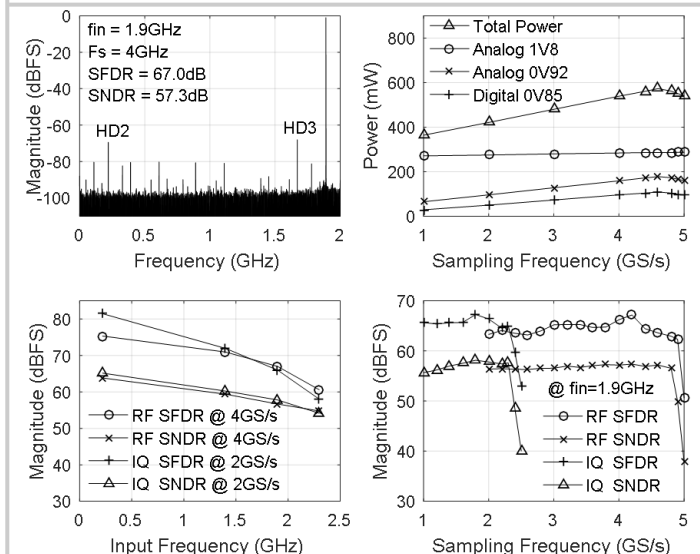


Figure 16.1.5: Measured dynamic performance and power dissipation.

	This Work	[1]	[2]	[3]	[4]
Architecture	Pipe-SAR	Pipeline	Pipeline	Pipeline	Pipe-SAR Hybrid
Technology (nm)	16	16	65	28	28
Fs (GS/s)	4.0	4.0	4.0	5.0	5.0
Interleaving	8x	4x	16x	2x	2x + 8x
Resolution (bits)	13	13	---	14	10
Power (mW)	513	300	2200	2300	150
SNDR (dB) @ peak	63.8	60.0	61.0	63.0	57.0
SNDR (dB) @ Nyq.	57.3	56.0	55.5	58.0	52.2
SFDR (dB) @ Nyq.	67.0	68.0	64.0	70.0	58.5
FoM _{Walden} @ Nyq. (fJ/conv-step)	214.2	145.5	1130.0	708.7	90.1
FoM _{Schreier} @ Nyq. (dB)	153.2	154.2	145.1	148.4	154.4
Area (mm ²)	1.04	0.34	12.0	14.4	0.45

Figure 16.1.6: Performance summary and comparison to prior works.

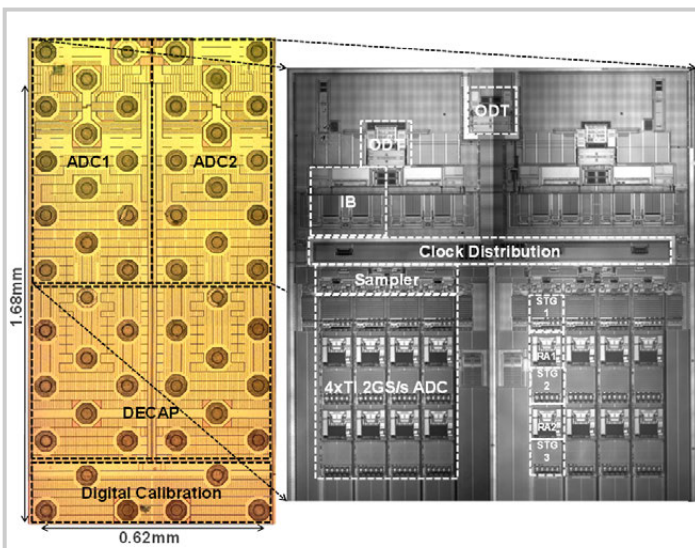


Figure 16.1.7: Die micrograph.

16.3 A 330mW 14b 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz

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Direct-RF synthesis has gained increasing attention in recent years [1] [2] as it simplifies the transmitter system by eliminating the intermediate frequency stage. It also offers the opportunity to address the extensive range of cellular bands with the same architecture and building blocks. Direct synthesis of carriers in the 5 to 6GHz unlicensed bands remains a challenge for RF-DACs operating in the 1st Nyquist band, as sampling rates in excess of 12GS/s are required. A more power efficient way to synthesize directly these frequencies is to use wideband mixing-DACs, which increase the output power in the 2nd and 3rd Nyquist bands [3]. In [3] the mixing is done using the quad-switch configuration, which doubles the number of switches and drivers, directly impacting the overall DAC width. In [4] the mixer is inserted in-line between the current cell switch and the output cascode, which requires additional headroom in the output stage. Both implementations impact the overall performance and power of the DAC even when the mixing operation is not used.

This work presents an alternative implementation of the mixing-DAC using the traditional current switching cell. The mixing is realized in the data path, enabling full utilization of the DAC analog bandwidth across 1st, 2nd and 3rd Nyquist zones without compromising performance. This dual-mode RF-DAC is manufactured in a 16nm FinFET process and demonstrates ACPR better than -70dBc in a 20MHz channel centered at 5.2GHz while dissipating a total power of 330mW including shared biasing, clock receiver and clock distribution.

Figure 16.3.1 depicts the overall architecture of the current-steering DAC. The incoming data is decoded to match the 6-8 unary-binary segmentation. The randomized unary and binary data are serialized at the output sample rate of the DAC using a 4:1 ratio. Dummy-data is generated in the next block, which ensures data-independent switching currents [5]. The data and dummy-data drive the main and dummy bit-slices made of 3 differential latches. The final latches implement an optional XOR mixing function between clock and data, and drive the current cells, which deliver an aggregate current of 20mA. The output current is carried to the 50Ω on-die termination through a 1.7nH shunt inductor, which pushes out the analog bandwidth by 55%.

The final differential latch needs to accomplish both the critical retiming of data in the normal mode and the XOR of data and clock in the mixing mode. In both modes variability of clock to output delay can significantly degrade high-frequency linearity and should thus be minimized. The chosen implementation of this mixing latch is shown in Fig. 16.3.2. In normal mode, switches marked S are closed and Smix switches are open. On the rising edge of the clock, switches S1 connect the complementary input to internal latch nodes INT+ and INT-, and through inverters I1 to the output. Simultaneously, switches S2 sample the inverted input on MEM+ and the input on MEM-. On the falling edge of the clock, switches S1 and S2 open and switches S3 and S4 close: S3 configures inverters I2 as a memory cell while S4 confirms the previously sampled value of INT+ and INT-. The mixing operation is similar except that, as Smix closes and S opens, nodes MEM+ and MEM- are charged to the input and inverted input respectively in the high clock phase. As a result, at the falling edge of the clock INT+ and INT- change polarity thus achieving the desired XOR operation. In normal mode the critical rising clock to output path only contains switches S1 and inverter I1. In mixing mode, S1 and I1 still determine rising clock to output delay but the falling clock to data delay is determined by S4 and I1. All of these transition times are only subject to variability of a switch and inverter, as is the case in a conventional differential latch. As a result, there is no penalty to timing variability due to implementation of the mixing mode. The few added inverters and switches outside of the critical timing paths do not meaningfully affect performance or power in 16nm technology.

The layout in the 16nm FinFET process is critical in order to achieve high performance. The final retiming cell and the current-steering cell metals are implemented to ensure metal mask misalignments, introduced by double patterning, do not add timing mismatch between the complementary paths of each cell and between cells. Star routing is used in power and ground grids of the data and the dummy-data paths to ensure matched voltage drop. The clock tree is implemented using a common buffer driving local buffers shared between pairs of cells in order to achieve the lowest time skew mismatch while still meeting electro-migration rules on all metals. The device finger-count in the unary current-steering cell is chosen to allow optimal scaling of the three MSB binaries. However, the five LSB binaries use smaller finger widths, which results in imperfect binary weighting of the charge injection when switching. The scaling of the metallisation is also done to attain the required time skew alignment and meet the required NSD. The current source is sized to achieve 12b matching, which also allowed the desired flicker noise performance to be achieved despite the degradation of this parameter in FinFET devices.

All presented measurements are carried out with the sampling frequency of the DAC set to 6881.28MS/s and the internal full-scale current set to 20mA. No correction for insertion loss of the test setup has been made, which is estimated at 2.6dB at 5.2GHz. Figure 16.3.3 illustrates the measured output of the DAC in both normal and mixing mode when driven by broadband noise data. The

frequency response shows $\frac{\sin(\frac{\pi f}{f_s})}{(\frac{\pi f}{f_s})}$ dependency in normal mode and $\frac{\sin^2(\frac{\pi f}{2f_s})}{(\frac{\pi f}{2f_s})}$

in mixing mode, as expected. Insertion loss and impedance mismatch further modify the transfer functions. The output power is maximized in normal mode when operating in the 1st Nyquist band while the mixing mode gives higher output power when synthesizing frequencies in the 2nd and 3rd Nyquist bands. Figure 16.3.4 (top) shows the measured ACPR in a 20MHz channel synthesized at 5.2GHz in both modes. In mixing mode, the ACPR and NSD are -70.8dBc and -160.2dBm/Hz respectively and the output power is increased by 8dBm compared to normal mode. In this configuration, the total measured power consumption is 330mW, which includes all blocks depicted in Fig. 16.3.1. Figure 16.3.4 (bottom) illustrates the full Nyquist spectrum of the DAC in mixing mode when generating a 2-tone signal at 5.2GHz. IM3, SFDR and output power as a function of output frequency are reported in Fig. 16.3.5. In normal mode, IM3 and SFDR are better than -71dBc and 62dBc respectively over the full 1st Nyquist band. In mixing mode, IM3 and SFDR are better than -65dBc and 59dBc respectively over the full 2nd Nyquist band. Finally, Fig. 16.3.6 summarizes the performance of the RF-DAC and shows a comparison with prior art.

References:

- [1] G. Engel, et al., "A 16-bit 10Gsp/s current steering RF DAC in 65nm CMOS achieving 65dBc ACLR multi-carrier performance at 4.5GHz Fout," *IEEE Symp. VLSI Circuits*, June 2015.
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- [4] E. Bechthum, et al., "A Wideband RF Mixing-DAC Achieving IMD < -82 dBc Up to 1.9 GHz", *IEEE JSSC*, vol. 51, no. 6, pp. 1374-1384, June 2016.
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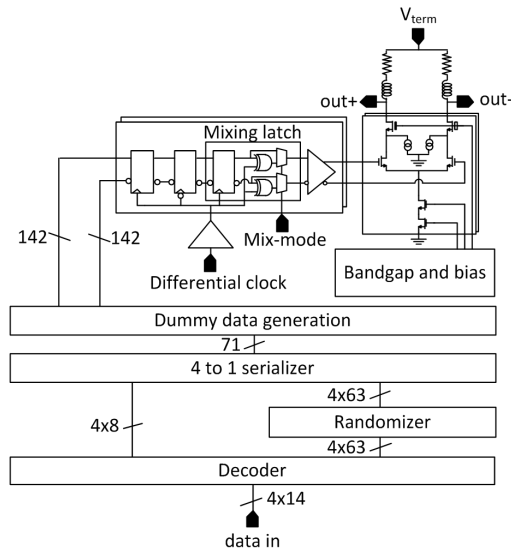


Figure 16.3.1: Block diagram of the mixing-DAC.

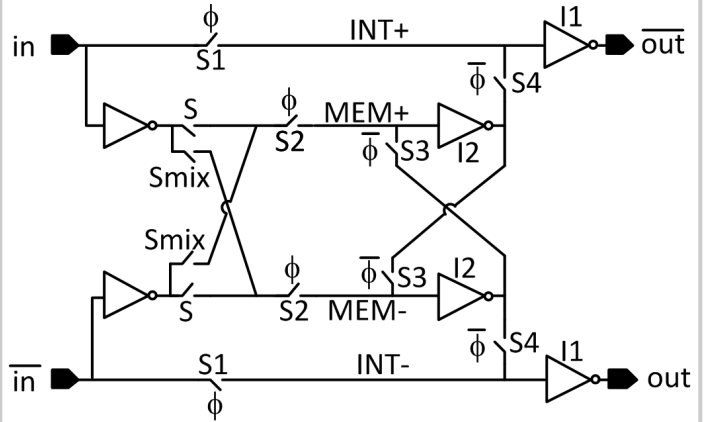


Figure 16.3.2: Mixing latch.

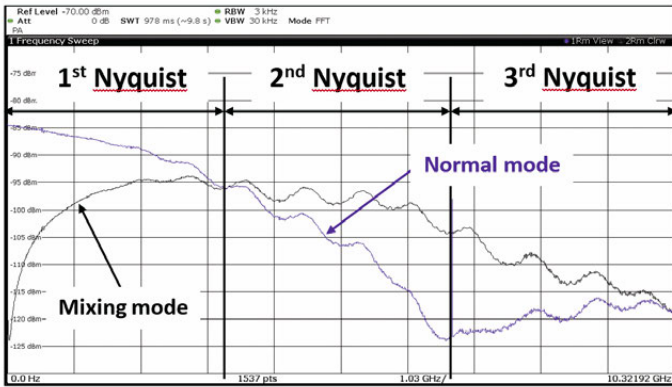


Figure 16.3.3: Transfer function of the RF-DAC in normal and mixing mode.

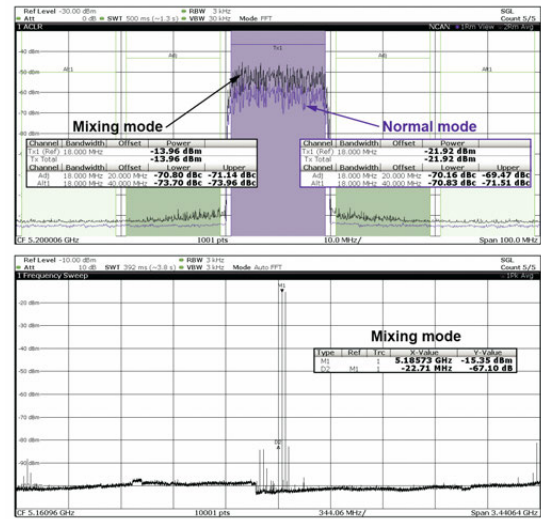


Figure 16.3.4: 20MHz channel ACPR at 5.2GHz in both modes (top). 2-tone Nyquist spectrum at 5.2GHz in mixing mode (bottom).

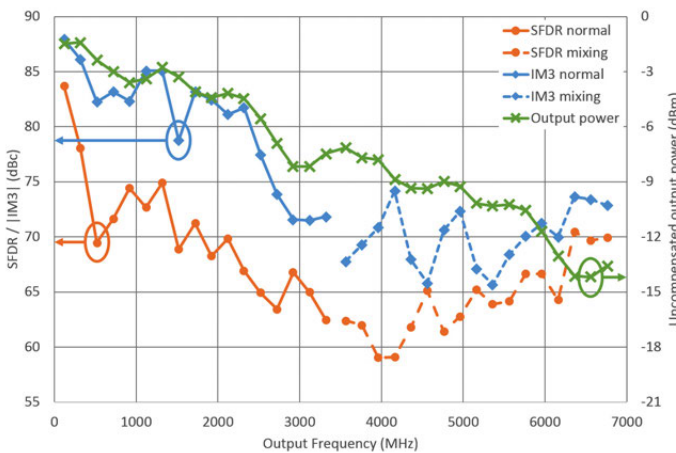


Figure 16.3.5: IM3, SFDR and uncompensated output power vs output frequency.

		This work	Engel [1]	Ravinuthala [2]	Bechthum [4]			
Process node	nm	16	65	40	65			
Sample rate	GS/s	6.8	10	8.9	1.75			
Effective Nyquist Bw	GHz	3.4	5	4.45	0.875			
Core power	mW	<330	800	1200	380			
F_{out}	GHz	1.9	2.7	4.1	5.2	4.5	2.9	4.1
20MHz channel ACPR@F_{out}	dBc	-76.5	-74	-72	-70.8	-65	-71	-73
IM3@F_{out}	dBc	-82	-74	-74	-67	-	-69	-62
SFDR@F_{out}	dBc	68	63	59	65	-	55	63
Core area	mm ²	<0.855	-	-	-	-	-	1.6

Figure 16.3.6: Summary of the RF-DAC performance and comparison with prior art.

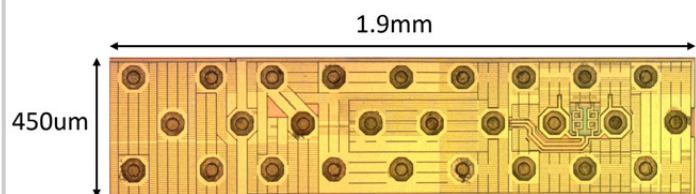


Figure 16.3.7: Die micrograph and dimensions.