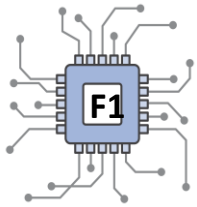
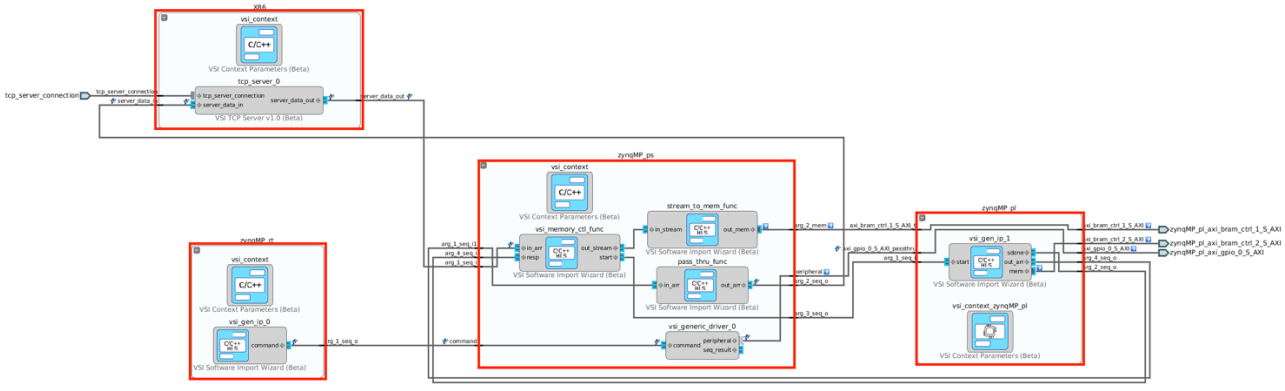
Visual System Integrator for Amazon AWS F1



System View Inc announces the availability of their intuitive graphical programming environment "**Visual System Integrator**" for developing applications on AMAZON's AWS F1 clusters.

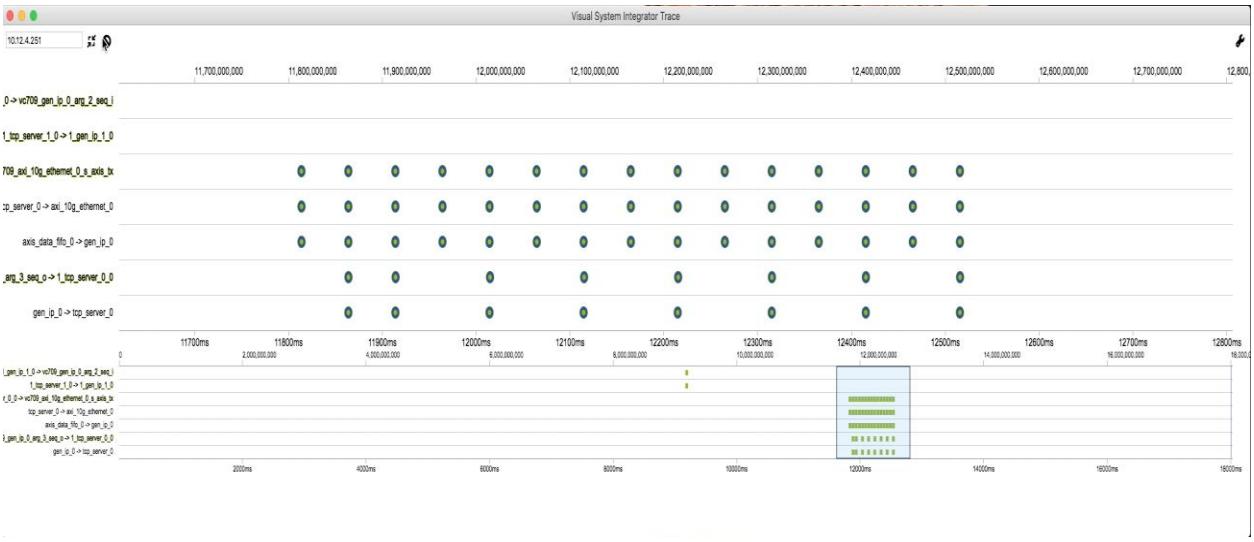
Easily program the AWS F1 FPGAs using C/C++ code.

Use VSI's powerful Software Import Wizard to import existing C/C++ functions, drag and drop them to FPGA's or CPU, connect them to represent the application Data Flow; press "Generate System" and let VSI system compiler create the complete system for you.



VSI generated runtime & data transport hardware, work in unison to transport the data between blocks executing in CPU and FPGA and between FPGA and FPGA.

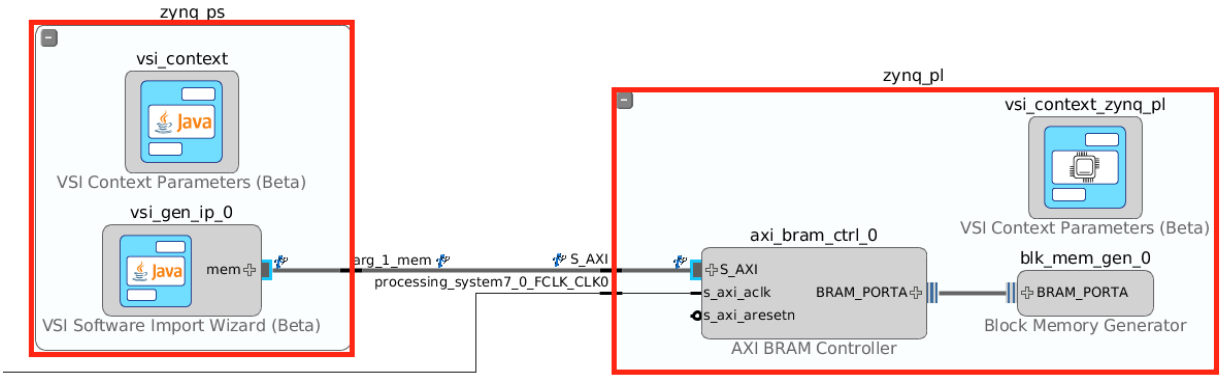
System level Trace



Use VSI's integrated system level ***"trace"*** application shows events across the entire system , both hardware and software , on a single timeline. With this capability the developer can quickly identify functional problems or performance bottle necks.

Access FPGA resources directly from JAVA or python

VSI software import wizard, can import Java functions. Use ***VsiDevice Class*** to access memory (HMC) or control devices in the FPGA.



The complete JAVA framework is available to the developer, use any of the existing frameworks like Apache STORM, HIVE, PIG, SPARK etc. and process data in FPGA(s).

Mix and Match

VSI's modular runtime environment allows developers to communicate between blocks developed in different languages. The developer can communicate with Blocks developed in RTL (Verilog, VHDL) from C, C++, Java or Python.

More Details .....

VSI supports AWS instances ***f1.2xlarge*** (one FPGA system), and ***f1.16xlarge*** (eight FPGA system), allowing you to utilize the full potential of this powerful heterogonous compute platform.

The AWS F1 version of **Visual System Integrator** comes with the platform definition for both ***f1.2xlarge*** and ***f1.16xlarge*** instances. The platform

describes the PCI/e connection between the FPGA boards and the CPU, the High-Speed Serial (SERDES) connection between the FPGA boards and the HMC memory controllers present in the FPGAs.

The developer can place the compute ***"block"*** in any of the FPGAs, the VSI system generator will transport the data using the appropriate connection. The developer can read/write data into the HMC memory of any of the connected FPGAs from the CPU using C, C++, Java or python, then invoke a processing function in the FPGA, the processing function in FPGA can be developed in C, C++, Verilog or VHDL.

Simulation Context

The AWS "Debug" platform includes a simulator "**context**". The VSI compiler creates a RTL simulation project for the block placed in this context. The user can choose the simulator (XSIM or QUESTA). The VSI runtime will transfer data between the Simulator and the rest of the system.

For more information, please visit our website
http://www.systemviewinc.com