

Zynq UltraScale+ RFSoc Product Tables and Product Selection Guide



		Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
Processing System (PS)	Application Processor Unit	Processor Core	Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5GHz				
	Real-Time Processor Unit	Processor Core	Dual-core ARM Cortex-R5 MPCore up to 533MHz				
	External Memory	Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB				
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core				
	Connectivity	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC				
		Static Memory Interfaces	NAND, 2x Quad-SPI				
	Integrated Block Functionality	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet				
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	PS to PL Interface	Power Management	Full / Low / PL / Battery Power Domains				
		Security	RSA, AES, and SHA				
	AMS - System Monitor	10-bit, 1MS/s – Temperature and Voltage Monitor					
		12 x 32/64/128b AXI Ports					
Programmable Logic (PL)	RF Data Converter Subsystem	12-bit, 4GSPS RF-ADC w/DDC	0	8	8	8	0
		12-bit, 2.058GSPS RF-ADC w/DDC	0	0	0	0	16
		14-bit, 6.554GSPS RF-DAC w/DUC	0	8	8	8	16
	Programmable Functionality	SD-FEC	8	0	0	8	0
		System Logic Cells (K)	930	678	930	930	930
		CLB LUTs (K)	425	310	425	425	425
	Memory	Max. Distributed RAM (Mb)	13.0	9.6	13.0	13.0	13.0
		Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0
		UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5
	Integrated IP	DSP Slices	4,272	3,145	4,272	4,272	4,272
		PCI Express® Gen 3x16 / Gen4x8	2	1	2	2	2
		150G Interlaken	1	1	1	1	1
		100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2
		AMS - System Monitor	1	1	1	1	1
		Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I	-1E, -1I, -1LI, -2E, -2LE, -2I, -3E	-1E, -1I, -1LI, -2E, -2LE, -2I, -3E	-1E, -1I, -1LI, -2E, -2LE, -2I	-1E, -1I, -1LI, -2E, -2LE, -2I, -3E
Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY, RF-ADC, RF-DAC	
D1156	35x35	214, 72, 208 4, 16, 0, 0					
E1156 ⁽¹⁾	35x35		214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8	214, 48, 104 4, 8, 8, 8		
G1517 ⁽¹⁾	40x40		214, 48, 299 4, 8, 8, 8	214, 48, 299 4, 16, 8, 8	214, 48, 299 4, 16, 8, 8		
F1760 ⁽¹⁾	42.5x42.5					214, 96, 312 4, 16, 16, 16	

1. Available in lidded and lidless stiffener ring packages.

Zynq® UltraScale+™ RFSoc Ordering Information



XC	ZU	##	D	R	-1	F	F	V	Footprint		E
Xilinx Commercial	Zynq UltraScale+	Value Index	Processor System Identifier D: Quad APU; Dual RPU	Engine Type R: RF Signal	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Highest	F: Flip-chip w/ 1.0mm Ball Pitch	F: Lid S: Lidless Stiffener	V: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (E, I)

E = Extended (Tj = 0°C to +100°C)
 I = Industrial (Tj = -40°C to +100°C)

Note: -L2E (Tj = 0°C to +110°C)

Export Control Disclaimer

Technical data provided to you by Xilinx may be subject to certain controls on its export, reexport and in-country transfer under applicable provisions of the U.S. Export Administration Regulations (“EAR”) administered by the U.S. Department of Commerce’s Bureau of Industry and Security and local trade regulations. You represent and warrant to Xilinx that you will not export, reexport or transfer the technical data provided by Xilinx to any other person or company without first obtaining any export license or other approval that may be required under applicable provisions of the EAR and local trade regulations, if any. Xilinx will provide reasonable assistance to you in connection with the classification of any controlled technical data on the Commerce Control List of the EAR, but you are solely responsible for the classification per any local trade regulations, for filing any applications, and obtaining any licenses or other approvals, that may be required in order for you to export, reexport or transfer in-country any controlled technical data you may receive from Xilinx to any other person or company.

XMP105 (v1.3)