PlanAhead Release Notes

What's New in the 11.1 Release

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Table of Contents

What's New in the PlanAhead 11.1 Release

This document provides an overview of the new features and functionality included in the PlanAhead™ 11.1 release. It will also highlight known features to be made available in upcoming 11.*x* incremental releases.

This document assumes that users will upgrade to ISE® 11.1 at some point. However, users electing to use previous ISE versions will still see significant benefits in migrating to PlanAhead 11.1, as support is available for versions of ISE 6.1i and later.

For more information, please refer to the *PlanAhead 11.1 User Guide* or contact the Xilinx Technical Support. For contact information, visit www.xilinx.com/support

Device Support

PlanAhead 11.1 fully supports all of the available Virtex® -4, Virtex-5 and Spartan® 3 FPGA devices. Virtex, Virtex-II, Virtex-II Pro and Spartan 2 device family support has been removed from ISE 11.1 software. ISE software version 10.1 or earlier should be used to design with those devices.

As new devices are introduced, they will be made available in PlanAhead through minor update releases. It is advisable to remain current with the PlanAhead update releases using the Xilinx Update capabilities. Update releases are distinguished by the last digit in the release number (11.2, 11.3, etc.).

PlanAhead 11.1 offers support for the following device families:

Virtex-5 TXT	Spartan-3A DSP
Virtex-5 FXT	Spartan-3AN
Virtex-5 SXT	Spartan-3A
Virtex-5 LXT	Spartan-3E
Virtex-5 LX	Spartan-3
Virtex-4 SX	
Virtex-4 LX	
Virtex-4 FX	

Installation and Licensing

All of the Xilinx® software tools have migrated to now use FlexLM licensing with the 11.1 release. Please refer to the *ISE 11.1 Release Notes and Installation Guide* for more information about installing the software, obtaining licenses and configuring the license manager.

Incremental Releases

Incremental PlanAhead Update releases will be made available using the existing *Xilinx Update* mechanism. Running *Xilinx_Update* will alert users of new PlanAhead releases and prompt to download and install the updates.

PlanAhead is now included with ISE Design Suite

Xilinx has made the full set of the powerful PlanAhead capabilities available to all ISE Design Suite users by introducing PlanAhead as a part of the standard 11.1 ISE release. It is no longer an additionally priced option. The PlanAhead software is automatically installed with the 11.1 ISE Design Suite.

After installation, Windows users can use the PlanAhead Desktop icon or Windows Start menu to invoke PlanAhead. Linux users should run the settings script or add the PlanAhead install *bin* directory to the search path. The *planAhead* command is used to invoke the tool.

For more information about the PlanAhead features, please refer to the *PlanAhead User Guide, PlanAhead Tutorial* or *What's New* section of the *11.1 ISE Design Suite Release Notes and Installation Guide*.

Project Navigator Integration

PlanAhead is now integrated with the ISE 11.1 Project Navigator design environment. It replaces the current PACE I/O pin planning tool and the previous ISE floorplanning tools.

PlanAhead will be called from Projnav when these 4 specific processes are invoked. When called from these processes, the design views and functionality of PlanAhead are limited to those required to fulfill the process (e.g pin planning pre-synth, vs. floorplanning post-synthesis). This simplifies the presentation of the data, reduces the complexity of the tool, and makes it easier to learn and complete each of the process steps. When Project Navigator invokes the PlanAhead environment, it is referred to as ISE Integration mode. The UCF constraint file referenced in the Project Navigator project is back-annotated based on any changes made to the design in PlanAhead when PlanAhead is closed or the project saved.

Refer to the *PlanAhead User Guide* for detailed information about the integration process as well as information about migrating from PACE or the ISE floorplanners. There is also a document titled *Introduction to Using PlanAhead with Project Navigator* that is presented in a dialog when PlanAhead is invoked from Projnav. It contains high level information about the integration.

New PlanAhead Features

I/O Pin Planning

PlanAhead 11.1 includes several enhancements to the PinAhead environment, as described below.

Alternate Compatible Devices

For Virtex-5 devices, PlanAhead 11.1 allows you to specify alternate parts during I/O pin planning. The alternate devices must be of the same physical package. PlanAhead will place I/O prohibits on the unbonded I/O pads that can not be shared across the various devices specified. This ensures that the I/O pin assignment will work across the devices selected. It is recommended to also use the *Run DRC* menu command/toolbar button on the target devices.

Importing I/O Ports Improvements

Several improvement were made to enable more flexibility while importing I/O Ports into PlanAhead 11.1.

- You can now import a User Constraint File (UCF) with I/O port definitions, I/O standards and I/O constraints into an empty PlanAhead Project to begin I/O pin planning without RTL or a synthesized netlist. The Port direction will not be defined as it is not included in UCF syntax. You can use the *Set Direction* popup menu command to define I/O Port direction.
- You can import ISE pad file CSV format files into PlanAhead to begin I/O pin planning.
- The imported CSV file can now contain additional columns of user specified information. PlanAhead will import, display, maintain and export these fields and their values. You can modify the field values while in PlanAhead. This feature enables you to have custom user specified information in the Package Pins list that is maintained throughout the I/O pin planning process using PlanAhead.

New DRCs

Many new I/O related DRCs have been added to PlanAhead 11.1. Please review the *I/O Pin Planning* chapter of the *PlanAhead User Guide* for information about the various I/O DRCs.

Miscellaneous PinAhead Features

1. PlanAhead now enables users to create differential I/O pairs. The *Make Diff Pair* command and the *Split Diff Pair* popup menu commands can be used to create and remove differential pairs. You are prompted to define the Positive and Negative signals for each pair.
2. The *Fix Instance* and *Unfix Instance* commands were renamed to *Fix Port* and *Unfix Ports* when I/O Ports are selected.

3. The I/O Ports and Package Pins table views can now be exported to a Microsoft Excel (xls format) spreadsheet using the *Export to Spreadsheet* popup menu command.
4. I/O Ports can be added to or removed from existing I/O Port Interfaces using the *Assign to Interface* or *Unassign from Interface* popup menu commands.

RTL Creation

The PlanAhead RTL environment contains HDL Source file management, an HDL Editor, RTL elaboration with RTL analysis including RTL netlist, hierarchy and schematic views as well as resource estimation, and lint-style DRC checks for power and performance. It has been enhanced in the 11.1 release and now also supports logic synthesis and implementation.

Importing Sources

PlanAhead projects can be created using Verilog, VHDL or both as the sources. You can now specify VHDL Libraries for files as they are imported. It is also much easier to use the enhanced Sources view to select multiple VHDL source files and set the library on them all simultaneously.

XCF format configuration files for XST synthesis can also be imported as source. They can be modified using the RTL Editor view.

NGC format core files can be imported as sources. They are copied into the various synthesis and implementation run directories.

Sources View Enhancements

The Sources view has been enhanced to display the source type, location, library and whether the source file is copied locally into the Project directory. The view can be configured to group and display the files by source type, by source root location or in a flat list.

Source files can be enabled or disabled for elaboration or synthesis by using the *Enable Source Files* or *Disable Source Files* popup menu commands. The capability allows you to experiment with various design configurations within the same Project.

The Sources view can be exported to a spreadsheet by using the *Export to Spreadsheet* popup menu command.

Importing Source Directories

Entire directory trees can be added to RTL projects. All currently supported file types of sources will be added to the project when selecting this option in the new project creation or add source wizards. All directories will be recursively searched for these sources below the specified directory.

RTL Editor

Several enhancements have been made to the RTL Editor to better display the various RTL constructs. The cross selection of various logic objects has also been improved.

Two commands have been added to enable quick RTL location for selected objects. Using the *Show Source* or *Show Definition* commands will highlight the specific logic code or the logic instantiation in the RTL Viewer for the selected logic object types.

RTL Analysis

RTL analysis can be performed by first elaborating the RTL netlist using the *Run Elaboration* command. Elaboration is a very quick technology mapping of RTL to primitives for the purposes of viewing schematics, resource estimation, and debugging RTL. It is not intended to have perfect correlation to the final synthesized netlist, as this would require the runtime of a full synthesis engine. It is an optional step in the synthesis and implementation process.

RTL Elaboration

PlanAhead 11.1 leverages the RTL parser supplied by Verific®. This widely used solution elaborates the RTL and performs basic legality checking. Issues with RTL constructs are displayed and cross-probable in the Elaboration Results view. Improvements in the elaboration process including accuracy, speed and memory allocation have been made in PlanAhead 11.1.

RTL Schematic Exploration

Once the RTL Source files have been elaborated, PlanAhead analysis features are made available. The Schematic view can be invoked on any selected logic and interactively expanded and explored. All of the views work very similarly to their PlanAhead counterparts that use the synthesized netlist data. The schematic representation of the RTL logic including symbols and logic inference has been improved in the 11.1 release.

Resource Estimation

Once the RTL is elaborated, estimations of the resources required are provided to help users select a target device and to get a sense of the size of their designs. These are early estimations based on RTL only and may change after synthesis and implementation. These accuracy of the resource estimation has been improved in the 11.1 release.

RTL DRCs

PlanAhead 11.1 now contains several RTL based DRCs. These checks are designed to provide guidance for performance or power optimization. They will highlight areas of the RTL source code that could present logic error conditions or that could be modified for improved performance. Refer to the *RTL Creation and*

Analysis section of the *PlanAhead User Guide* for more information about the types of RTL checks included.

Debugging with ChipScope

One of the other big improvements in PlanAhead 11.1 is the integration of the ChipScope core insertion and debug capability. You can now select signals for probing, insert and compile the ChipScope ILA or ICON cores into a synthesized netlist, and launch the ChipScope Analyzer on completed runs with bitstreams. The integration allows you to configure the cores prior to implementation and enables experimentation with implementation options. You can interactively explore the core logic with the Schematic view and to analyze and floorplan the logic resources used by the cores.

RTL Cores

PlanAhead 11.1 now recognizes ChipScope cores inserted in the RTL logic

Inserting and Compiling the ILA Cores

You can select nets to probe with ChipScope cores using either the Netlist, Schematic or Find Results views. The “Unconnected” nets are displayed in the ChipScope view.

A *Set up ChipScope* wizard is available to walk through the process of selecting nets for analysis and configuring the cores. Once the *Set up ChipScope* command has been run, PlanAhead will trace the logic for the clock signal driving the signals and display it in the ChipScope view. PlanAhead will automatically insert as many cores as are required to satisfy the signals selected.

Once the cores are configured, PlanAhead will call the appropriate ChipScope commands to compile the cores and insert them into the logical netlist prior to implementation. Each implementation run will then contain the core logic. The PlanAhead Schematic view can be used to analyze the inserted core logic.

The netlist can then be updated or re-synthesized and PlanAhead will attempt to keep the probed core signals intact. A report is issued if probed signals changed or were affected during the netlist modification.

There are many core configuration, reporting and analysis capabilities included in the PlanAhead integration with ChipScope. Please refer to the *Debugging the Design with ChipScope* chapter of the *PlanAhead User Guide* for more information.

ChipScope DRCs

Several DRCs have been added to validate that the core configuration and insertion has been performed successfully.

Launching the ChipScope Analyzer

Once an implementation run has completed and the *bitgen* command has been run to create a bitstream, the ChipScope Analyzer can be launched to debug the design. Simply select the completed run and use the *Run ChipScope Analyzer* command.

Logic Synthesis and Implementation

The addition of a logic synthesis environment and front to back process is one of the biggest additions to PlanAhead in the 11.1 release. You can now import RTL sources, synthesize the logic, implement the synthesized netlist, analyze the implementation results, floorplan and experiment with implementation options and generate bitstreams. It is going a long way toward providing a comprehensive front to back design environment and solution.

Design Flow and Project Management Improvements

The way in which PlanAhead manages the design flow and data has changed in 11.1 to accommodate experimentation with multiple synthesis and implementation runs simultaneously. Previously, PlanAhead Projects consisted of a single imported netlist. You could create multiple Floorplans for experimentation, which were basically constraint sets that all leveraged that single version of the netlist. Creation of a Floorplan was always required and the netlist was always loaded into memory during a PlanAhead session.

In 11.1, you can experiment with multiple synthesis runs using different synthesis strategies. This process results in multiple netlists being created and stored within the PlanAhead Project. PlanAhead now enables you to interactively load the various versions of the netlist into the environment for analysis, I/O pin planning or floorplanning. Only one netlist version can be loaded at a time using the *Import Run Results* command. You are prompted to load the netlist for analysis, I/O pin planning or floorplanning and the appropriate view layout is initiated.

Since logic synthesis is performed prior to physical implementation, creation of a Floorplan is not required to create or analyze synthesis runs. You are prompted to create a Floorplan only when physical constraint modification is required or performed.

Creating Synthesis Runs

The interactive logic synthesis environment now utilizes the ExploreAhead environment that was used for implementation only in previous releases. The term “ExploreAhead” has been removed from the tool interface and documentation. It is now referred to as the PlanAhead logic synthesis and implementation environment.

The PlanAhead 11.1 synthesis and implementation environment enables you to configure, launch and monitor multiple synthesis runs using the Xilinx XST synthesis tool. You can define reusable “strategies” for synthesis runs. A Strategy consists of a set of options and option values to achieve a certain design objective. As an example, you might create strategies for power, performance or area optimization. You’d then assign these strategies to individual runs and launch them simultaneously or serially.

The *Run Synthesis* command can be used to create and launch an individual synthesis run with an applied strategy. The *Run Multiple Strategies* command can be used to create and launch multiple synthesis runs using multiple strategies.

The Design Runs view displays the runs created allowing you to monitor the status and view the results. The XST report file can be viewed as well as the FMax and SLICE utilization statistics.

Run result netlists can then be imported into PlanAhead to analyze the logic or to view resource statistics. The netlist can also be used to create a PlanAhead floorplan for post-synthesis I/O pin planning, design analysis, floorplanning and implementation.

Creating Implementation Runs

Implementation runs can be created directly from the synthesized run netlist or from within Floorplans. Creating Floorplans allows you to experiment with various logical or physical constraints or alternate devices. You can define reusable “strategies” for implementation runs. As an example, you might create strategies for the various map logic optimization options or par effort levels. You’d then assign these strategies to individual runs and launch them simultaneously or serially.

The *Run Implementation* command can be used to create and launch an individual implementation run with an applied strategy. The *Run Multiple Strategies* command can be used to create and launch multiple implementation runs using multiple strategies.

In previous releases, a Floorplan was required to be able to create runs or to analyze results. The constraints defined in the Floorplan were exported to the implementation tools. This capability still exists and works the same way for creating and launching runs from a Floorplan. However, you can now create and launch runs directly from a synthesized netlist without creating a Floorplan. You have the ability to define an external UCF for each run.

Runs can be imported into the PlanAhead environment for further analysis. The netlist, UCF constraints, placement and timing results are all imported into the PlanAhead environment for analysis. If you make any changes to the constraints,

you are prompted to save the changes as a Floorplan for future implementation or analysis purposes.

Double-clicking on a run will invoke the Import Run Results dialog to import the results.

Support for Remote Hosts

PlanAhead 11.1 provides the ability to run the implementation on remote hosts. This features uses the *ssh* command, which limits its availability to Linux users only. Users can define and configure a set of remote hosts using the *Tools > Options > Configure Remote Hosts* dialog. Upon launching runs, users can specify which machine to use for each run. A *Test* button is provided to ping the remote machines to ensure the machine can be logged into. There are some additional setup requirements for machines to utilize this capability. Please see the PlanAhead User Guide for information on configuring multiple remote execution hosts.

Importing ISE Results from Command Line Tools

A fourth option was added to the Create Project wizard to step through the process of importing ISE implementation results that were created outside of PlanAhead using the command line tools.

Design Analysis

Timing Analysis

The TimeAhead static timing analysis has been updated to better support Virtex-5 and some Virtex-4 designs. Accuracy has been improved over previous TimeAhead versions with certain logic constructs in those devices.

TimeAhead now allows you to specify an alternate speed grade to estimate the performance of your design in the various speed grades available for the target device.

The Timing Results view now categorizes the timing paths by constraint for results imported from TRCE. This includes results derived from TimeAhead or imported from *Trce*. The report also indicates whether the path is Setup or Hold related. The list of timing paths can be toggled to display a flat list as in previous releases or the new categorical constraint based list.

The Path report has been improved to now display clock skew. The format of the report has been consolidated to display information more effectively.

Tooltips have been added to the fields in the Timing report and the Path report to display long text strings such as Source and Destination paths without scrolling or resizing the views.

PlanAhead now supports importing *Trce* .twx format report files from ISE 11.1 and later. The path properties report also shows hyperlinks to timing parameters for cell delays to the online documentation in the device data sheet. Users may also search the device user guides manually for graphical representations of these timing parameters.

Searching for Objects

The *Find* command dialog now has a means to select which netlist to search for objects. If the RTL has been elaborated and a synthesized netlist is loaded, you can now select which netlist to perform the search.

Many new object types and filtering criteria have been added to the search dialog. There are too many to list here, but generally there is better control of search filtering based on primitive type and attributes. Experiment with the filtering menus in the Find dialog for more information.

New DRCs

Many new DRCs have been added to PlanAhead 11.1. Please review the *Analyzing the Design* chapter of the *PlanAhead User Guide* for information about the various DRCs.

Hierarchical Resource Statistical Reporting

You can now output spreadsheet reports of resource utilization statistics for any level(s) of the logic hierarchy. The Pblock and Instance Properties view now contain an *Export Statistics* Toolbar icon. It invokes a dialog allowing you to define the types of information to include in the report as well as how many levels of logic hierarchy to traverse and include in the report.

Floorplanning

Pblock Improvements

The underlying Pblock manipulation algorithms have been improved in PlanAhead 11.1 to fix issues with rectangle and range rendering during Pblock creation, resizing and moving operations. This enables more flexible and consistent Pblock and LOC constraint manipulation. Some of the improvements include:

- Users are prompted to adjust Pblock Range types as Pblocks are moved or reshaped over new device resources.
- Pblock graphics use shading techniques to indicated logic type ranges that are assigned in the Pblock.

Prohibit Sites

The ability to prohibit logic sites including CLBs, BRAM, DSP and I/Os from being used during implementation has been enabled in PlanAhead 11.1. It will display a red X on all prohibited sites from an imported UCF or when set in PlanAhead. To set it in PlanAhead, select one or more sites in the Device and use the *Set Prohibit* popup menu command. You can use the *Select Area* command to select a group of sites inside of a rectangle. . Similarly, you can clear Prohibits from selected sites.

Miscellaneous

1. The Main Toolbar has been simplified by moving some of the view specific Toolbar icons into the views that they interact with. The Device view now contains several new Toolbar icons for commands specific to the Device view.
2. The *Tools > Options > Shortcuts* configuration capability has been extended to now allow more flexible user defined shortcuts. This includes the ability to view specific shortcut keys. These user defined shortcut schemas are stored and retrieved from each users PlanAhead custom configuration file area.
3. The table type views such as the Timing Report, I/O Ports, etc, now have a search filtering mechanism to filter the listed set of objects. Select the magnifying glass Toolbar icon and enter any text string to filter the objects displayed in the view. There is an options menu next to the Search Field that allows you to define the table column for which to perform the search.
4. On Windows, PlanAhead Projects can now be opened from the Desktop by double clicking the Project files with .ppr extensions. On Linux, ppr files may be passed in as an argument to the PlanAhead command, and the project will be opened automatically.
5. PlanAhead now utilizes the C-based Tcl version 8.5 open source engine.
6. The planAhead.log and planAhead.jou files can now be viewed from within PlanAhead by selecting the *Tools > View PlanAhead Log File* or *Tools > View PlanAhead Journal File* commands.
7. The *Run Properties > Monitor* view can now be toggled to update the command status live as commands are running or to allow you to scroll back and browse results without the view continually updating. The "*Automatically update the contents of this view*" Toolbar icon can be used to toggle the behavior. This capability also exists when displaying the *planAhead.log* and *planAhead.jou* files.

Known Issues

1) Simultaneous Edits while using PlanAhead with Project Navigator

Users should be careful not to edit sources in Project Navigator while PlanAhead is invoked from Project Navigator. When PlanAhead is invoked, the netlist and UCF file sources are passed to PlanAhead. After making edits in PlanAhead, the UCF file(s) are passed back. If edits are made in Project Navigator while PlanAhead is invoked, changes may be lost.

Solution:

Make and save all changes in PlanAhead and exit the tool prior to modifying sources in Project Navigator.

2) Replace All in RTL Editor only replaces from insertion point

The *Replace All* command in the RTL Editor only replaces text occurrences from the cursor insertion point to the end of the document. It does not wrap around to the beginning of the file to perform replacements

Solution:

Place the cursor at the top of the file prior to using the *Replace All* command.

3) Protected Cores with netlist security attributes not imported

If the design contains cores with the netlist security attribute, they are not imported by PlanAhead. The module will appear as a block box in PlanAhead. However, the original core files will be copied to the run directories and implemented. Implementation results for those cores are also not imported into PlanAhead.

4) VREF DRC incorrect for DIFF_HSTL_1 and DIFF_HSTL_II_18 for Spartan3A

The Device Data Sheet and the PlanAhead DRC checks for these I/O standards are incorrect and may issue false errors.

Solution:

Ignore the DRC Errors.

5) Select Primitives command is slow when RTL sources imported into the Project

Solution:

Wait for the command to complete. Fixed in 11.2