

# Team Design Tutorial

## *PlanAhead Design Tool*

UG839 (v14.1) April 24, 2012

This tutorial document was last validated using the following software version: ISE Design Suite 14.1

If using a later software version, there may be minor differences between the images and results shown in this document with what you will see in the Design Suite.





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# Team Design Tutorial

The Team Design flow is a hierarchical design methodology that uses partitions to allow a large, complex design to be broken up into smaller logical blocks.

- These blocks can be implemented independently and simultaneously.
- This allows each block to be individually designed, implemented, and verified in context with the rest of the design.
- When all blocks are complete, the entire design is brought together in an assembly run in which results can be imported and preserved.

A Team Design flow team consists of:

- One team leader
- One or more team members

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## Tutorial Objectives

This tutorial provides an overview of the Team Design flow. In this tutorial, you will complete a design acting as a team leader and various team members. The objective of this tutorial is to familiarize you with partitions and the Team Design flow using the PlanAhead™ software.

## Project Setup

Initially, as team leader, you will:

- Define partitions on each team member block.  
Each team member block is a black box.
- Define Pblocks.
- Review existing physical and timing constraints.
- Synthesize an initial version of the design using Xilinx® Synthesis Technology (XST) incremental synthesis.
- Promote synthesis results for the Top partition.
- Run a Design Rules Check (DRC).
- Implement the initial design.
- Create PlanAhead projects for each team member.

## Team Member Work

When a PlanAhead project has been created for each team member, you will complete the work of each team member as follows:

- Update the project to include actual design files for the team member block.
- Synthesize the updated team member design while importing the Top partition  
Other team member blocks are black boxes.
- Implement the team member design.  
Other team member blocks are black boxes.
- Promote successful synthesis and implementation results to a location accessible by the team leader.

## Design Assembly

The team leader then assembles the design by importing the results from each team member project. You will:

- Assemble the design by importing the results from each team member project.
- Update the team leader project to include NGC files for each team member block.
- Set up implementation to import each team member block while implementing the Top partition.
- Verify design assembles while maintaining placement and routing results from each team member.

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## Software Requirements

You must have access to the ISE® Design Suite software to perform this tutorial.

Be sure that the PlanAhead tool is operational and the sample design data is installed before beginning the tutorial.

The PlanAhead tool, Version 14.x, supports partitions in RTL projects targeting Spartan®-6, Virtex®-6, and newer families.

For installation instructions and information, see the *ISE Design Suite: Installation and Licensing Guide (UG798)* at [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx14\\_1/iil.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/iil.pdf).

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## Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller xc7k70t design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

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## Tutorial Design Description

This tutorial uses an incremental synthesis flow to create separate netlist for each partitioned instance. These individual netlists are required for a team design flow.

The design used throughout this tutorial contains:

- A RISC processor
- FFTs
- Gigabit transceivers
- Two USB port modules (to be partitioned)
- An xc7k70tfbg676 device

This tutorial uses a small design to:

- Allow the tutorial to be run with minimal hardware requirements.
- Enable timely completion.
- Minimize the data size.

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## Locating Tutorial Design Files

Download the `PlanAhead_Tutorial.zip` file from the Xilinx website:

[http://www.xilinx.com/support/documentation/dt\\_planahead\\_planahead14-1\\_tutorials.htm](http://www.xilinx.com/support/documentation/dt_planahead_planahead14-1_tutorials.htm)

Extract the zip file contents into any write-accessible location.

The unzipped `PlanAhead_Tutorial` data directory is referred to in this tutorial as `<Extract_Dir>`.

The tutorial sample design data is modified while performing this tutorial. A new copy of the original `PlanAhead_Tutorial` data is required each time you run the tutorial.

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## Step 1: Opening a Project and Elaborating RTL

The PlanAhead design tool enables you to create several project types depending on where in the design flow the tool is being used. RTL sources can be used to create a project for development and analysis, synthesis, implementation, and bit file creation.

This tutorial uses an existing PlanAhead tool project, and focuses on the team design aspects in the software. You will not create a new design using the New Project Wizard.

### Opening the PlanAhead RTL Project

To open the PlanAhead RTL project:

1. Open the PlanAhead tool.
  - On Windows, select the Xilinx PlanAhead 14 Desktop icon, or select **Start > All Programs > Xilinx Design Tools > Xilinx ISE Design Suite 14.1 > PlanAhead > PlanAhead**.
  - On Linux, go to the <Extract\_Dir> directory and type **planAhead**.
2. From the Getting Started page, click **Open Project**.
3. Browse to <Extract\_Dir> and open the project file located at:

```
./Projects/project_TL/project_TL.ppr
```

The Project Manager view opens. You can view the design source files in the Hierarchy window. These files include:

- VHDL and Verilog files
- A User Constraint File (UCF) named top\_full.ucf. The UCF contains timing constraints and I/O pin locations.

### Elaborating Elaborated Design

Use the Elaborated Design view to define partitions in an RTL project. When the Elaborated Design view is opened:

- The RTL code is elaborated.
- The design hierarchy is displayed.

This is a pre-synthesized view of the design that is used to define partitions and create constraints.

To open the Elaborated Design view:

1. In the Flow Navigator, click **Open Elaborated Design**.

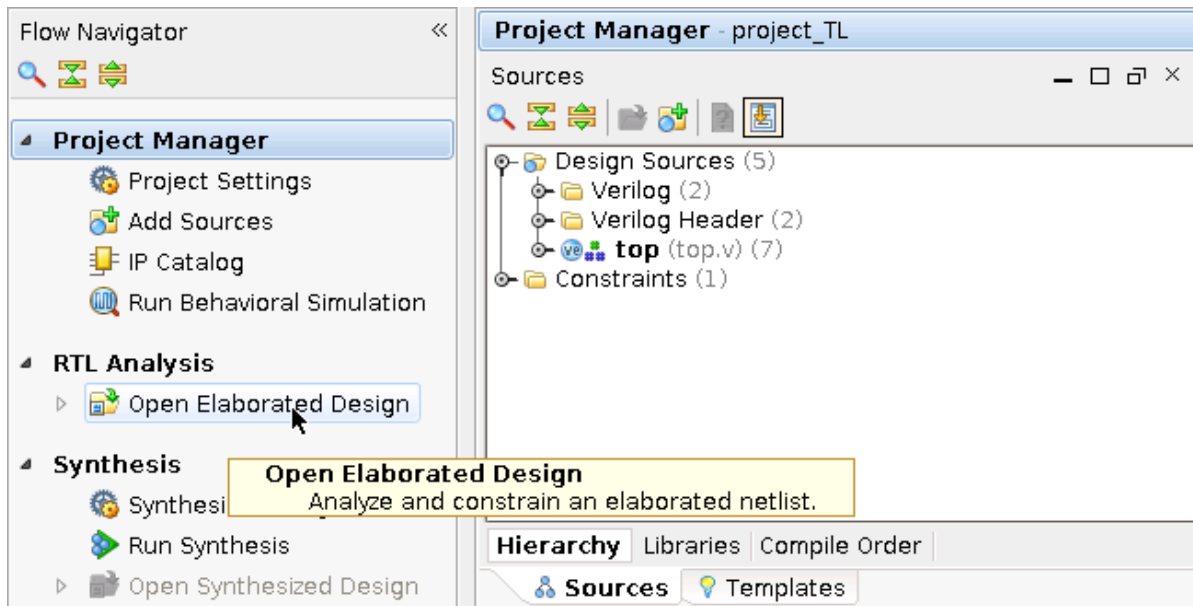


Figure 1: Opening the Elaborated Design View



---

## Step 2: Setting Partitions and Drawing Pblocks

The two **usbEngine** instances and the **cpuEngine** instance are all good candidates for partitioning for the following reasons.

- They are logically isolated from one another and do not benefit from optimizations with other blocks.
- They are timing critical blocks that can be developed independently and are beneficial to preserve once implemented.
- The interface timing in and out of these blocks are not critical as they are registered.

You can use the PlanAhead design rule checks to help identify modules that are good candidates for partitions.

You can floorplan partitioned instances just like any other instance. Creating Pblock (AREA\_GROUP) constraints can help achieve timing closure and improve runtime.

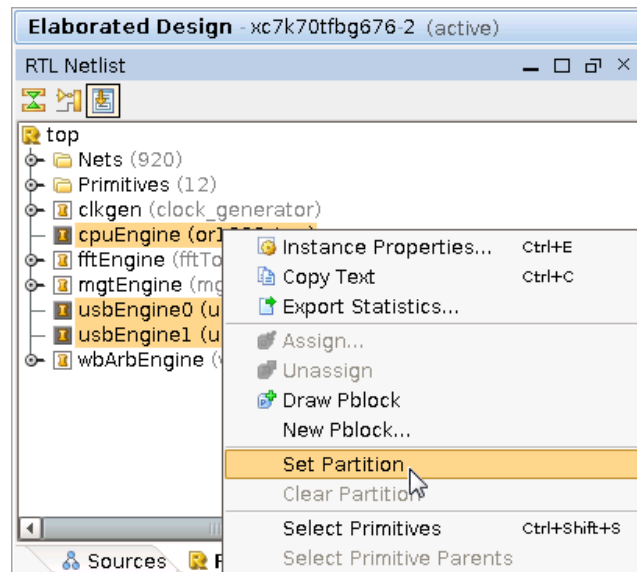
The steps below show you how to set partitions and create appropriate Pblock constraints for the team member instances. Pblocks are required in a Team Design flow for each team member partition.

### Setting Partitions on Team Member Instances

To set partitions on team member instances:

1. From the Elaborated Design view, click the **RTL Netlist** tab.
2. Press **Ctrl** and select:
  - **usbEngine0**
  - **usbEngine1**
  - **cpuEngine**

3. Right-click.
4. Select **Set Partition**.



**Figure 2: Setting Partitions on usbEngine and cpuEngine Instances**

Although three partitions are defined here, there are only two team members in addition to the team leader. Both **usbEngine** instances are managed by a single team member because there is only one set of Hardware Description Language (HDL) code associated with this module.

## Drawing Pblocks for the Team Member Partitions

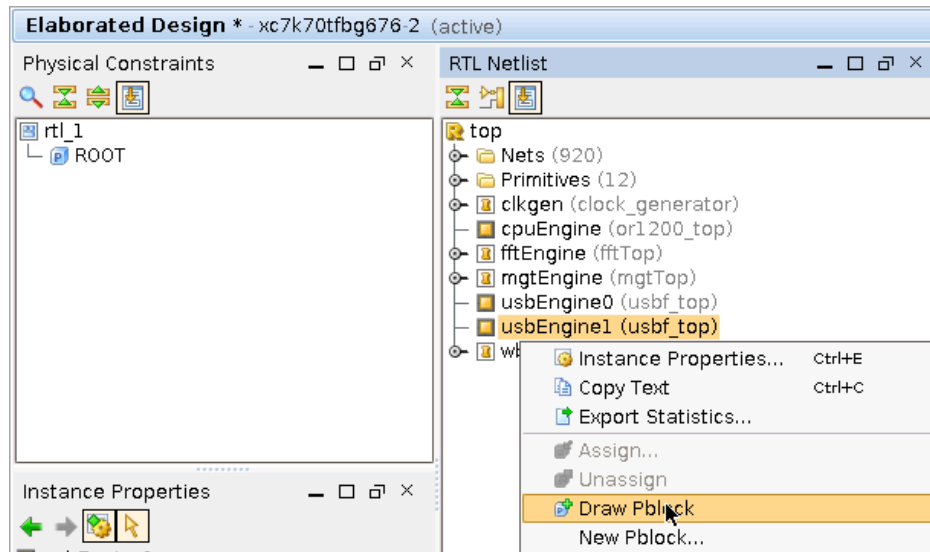
In this step, you:

- Define Pblocks.
- Review existing physical and timing constraints.

This step does not affect synthesis results. You could perform it post-synthesis in the Synthesized Design view instead.

To draw Pblocks for the team member partitions:

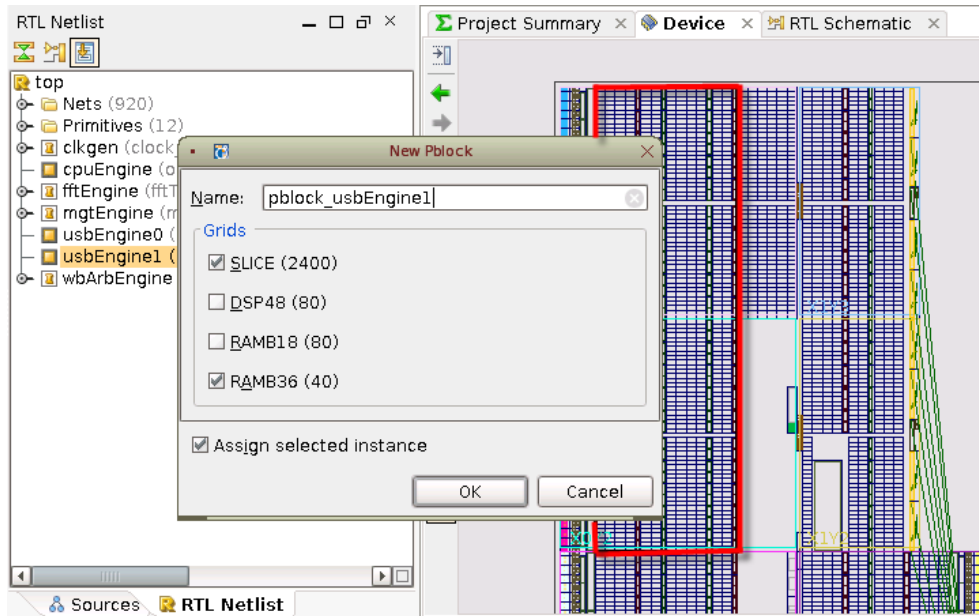
1. Change the layout to be Floorplanning by selecting **Layout > Floorplanning**.
2. From the RTL Netlist window, select **usbEngine1**.
3. Right-click and select **Draw Pblock**.



**Figure 3: Selecting the Draw Pblock Tool**

4. With the Draw Pblock tool active, move the cursor to the Device window.
5. Click the top-left corner of the device where the CLBs start (reference Figure 5 for completed view).

6. Drag down and to the right to create a rectangle covering most of the top-left quadrant of the device.



**Figure 4: Pblock Rectangle for usbEngine1**

7. In the New Pblock dialog box:
  - Verify that the SLICE and RAMB36 grids are selected.
  - Deselect other resources that are not needed.
  - Verify that the number of available RAMB36 is 40.

If the rectangle does not fully cover the region shown in the figure above (*Pblock Rectangle for usbEngine1*), the design may fail to place.

8. Click **OK**.
9. If the number of available resources are different than shown, adjust the size of the Pblock rectangle by selecting it and resizing.
  - SLICE (2400)
  - RAMB36 (40)
10. Repeat the steps above for **usbEngine0** in the bottom-left quadrant.

Only SLICE and RAMB36 (40 of them) are required for this block.

11. Repeat the steps above for **cpuEngine** in the bottom-right quadrant.

For **cpuEngine**, the Pblock contains all four ranges, and may be defined as clock regions X1Y0 to X1Y1 as well:

- CLOCKREGION\_X1Y0:CLOCKREGION\_X1Y1

Or as individual sites

- SLICE (2600)
- DSP48 (40)
- RAMB18 (80)
- RAMB36 (40)



**Figure 5: Completed Floorplan for Pblocks usbEngine0, usbEngine1, and cpuEngine**

---

## Step 3: Synthesizing and Implementing the Design

In the previous steps, you:

- Defined partitions on the elaborated HDL design.
- Created constraints.

In this step, you will:

- Run synthesis.
- Run DRC.
- Run implementation.

During synthesis, XST recognizes that the design has partitions, and runs the design through an incremental flow.

In this flow XST generates individual NGC files for each partition. In this design the top partition contains all logic in `top.v`, as well as all logic from hierarchical blocks that are not their own partition (**fftEngine**, **mgtEngine**, and **wbArbEngine**). All of logic from the top partition will be synthesized to `top.ngc`. Since the instances **usbEngine0**, **usbEngine1**, and **cpuEngine** are black boxes and contain no logic in this initial project, no NGC files will be generated for these partitions.

This tutorial uses an RTL project. For a bottom-up or third-party incremental synthesis flow:

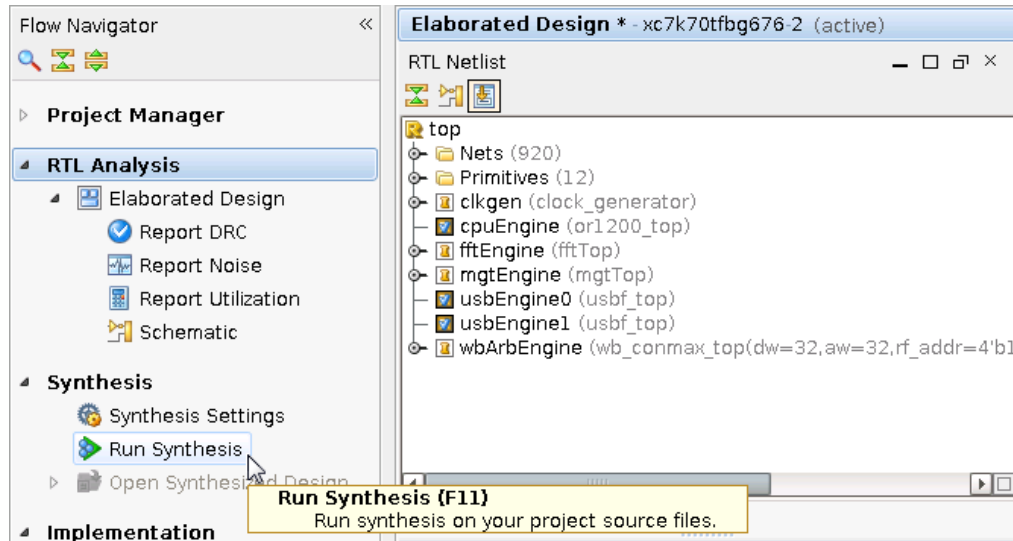
- Run synthesis outside the PlanAhead tool.
- Use a netlist project instead of an RTL project in the PlanAhead tool.

## Running Synthesis

This design uses default synthesis options.

To run synthesis:

1. In the Flow Navigator, click **Synthesize**.



**Figure 6: Launch XST Incremental Synthesis**

2. Before running synthesis, PlanAhead saves all partition and floorplan changes. If prompted to save your design, click **Save**.
3. After synthesis completes a Synthesis Completed dialog box will appear. You can either choose to **Open Synthesized Design**, or **Cancel** the dialog and open the Synthesized Design in the next step.

## Running DRC on Partitions

You can run a Design Rule Check (DRC) on the Elaborated Design, although the checks at this stage are limited. Xilinx recommends that you run a DRC on the post-synthesis design before implementation.

To check DRC, load the Synthesized Design view, and run partition-specific DRCs.

1. If not already open, open the Synthesized Design view by clicking **Open Synthesized Design** to in the Flow Navigator.

This loads the synthesis results and allows for additional DRC checking.

2. Click **OK** on the Undefined Modules dialog. It is expected to have black boxes in the design at this point.
3. In the Flow Navigator under Synthesized Design, click **Report DRC**.

4. From the Report DRC dialog box, deselect all rules except **Partition** and **Team Design**.

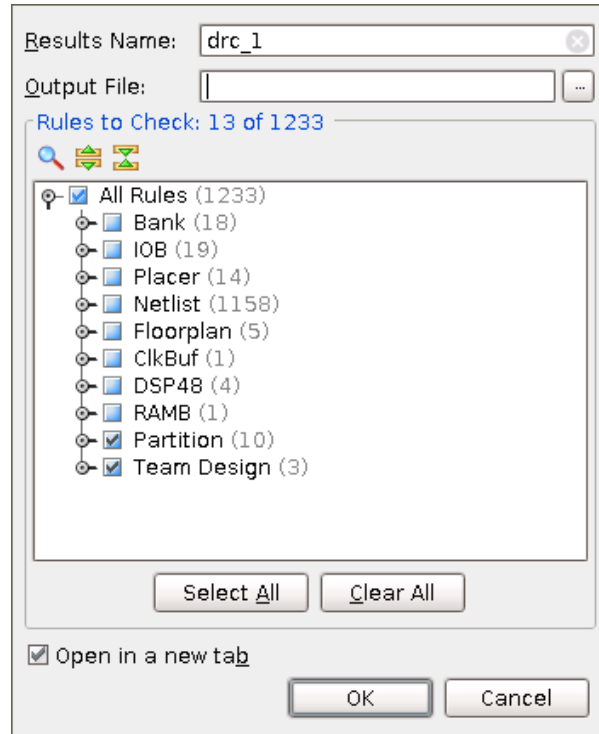


Figure 7: Run Partition Design Rule Checks

5. Click **OK**.

## DRC Messages

The PlanAhead tool can report the following message types for the DRC rules:

- Advisory
- Warning
- Error
- Fatal

In this case, the DRC returns several warning messages. Ignore them. The DRC messages are caused by the black boxes in the design.

In an actual design, investigate all DRC messages, and correct any serious issues.

## Running Implementation

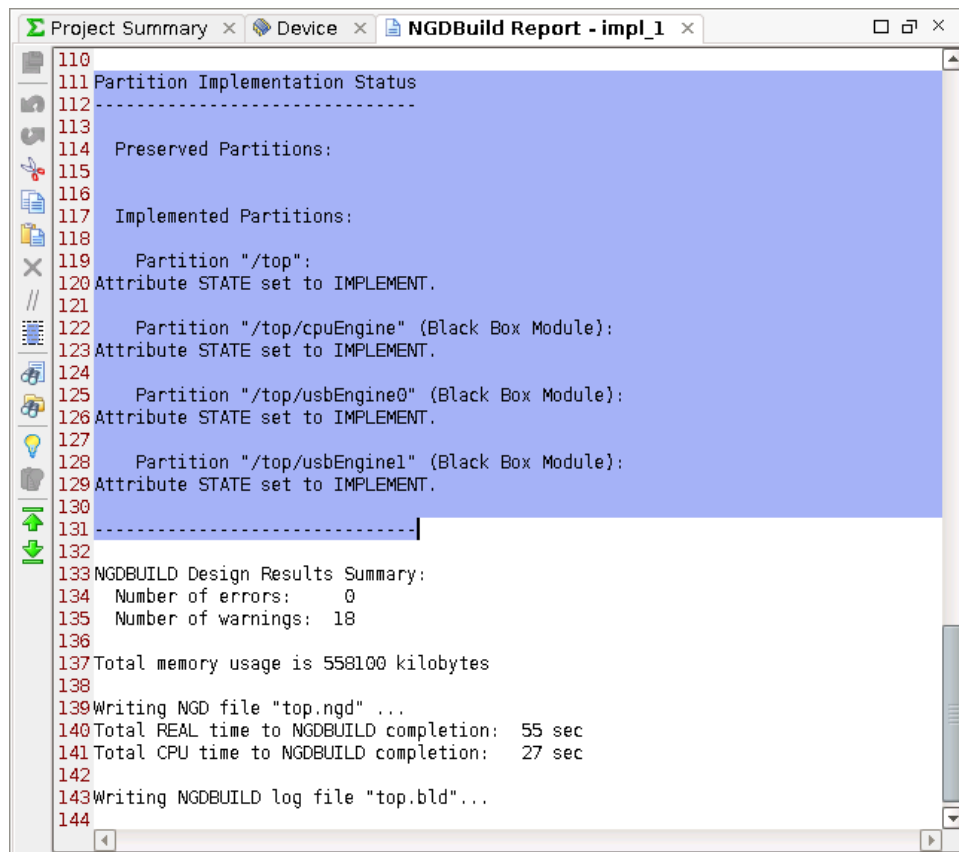
Before transmitting the design to each team member, the team leader may now run implementation to check that all timing and floorplan constraints are valid. Because the two



**usbEngine** instances and the **cpuEngine** instance are black boxes, no real useful implementation results are obtained.

To run implementation:

1. In the Flow Navigator, click **Run Implementation**.
2. Click the **Report** tab to see a list of all implementation reports.
3. As each process finishes, the related reports are available for review.
4. After NGDBuild finishes, double-click the **NGDBuild Report** to open the report.
5. Scroll to the bottom of the report file to review the partition information.



```
110
111 Partition Implementation Status
112 -----
113
114 Preserved Partitions:
115
116 Implemented Partitions:
117
118 Partition "/top":
119 Attribute STATE set to IMPLEMENT.
120
121 Partition "/top/cpuEngine" (Black Box Module):
122 Attribute STATE set to IMPLEMENT.
123
124 Partition "/top/usbEngine0" (Black Box Module):
125 Attribute STATE set to IMPLEMENT.
126
127 Partition "/top/usbEngine1" (Black Box Module):
128 Attribute STATE set to IMPLEMENT.
129
130 -----
131
132
133 NGDBUILD Design Results Summary:
134 Number of errors: 0
135 Number of warnings: 18
136
137 Total memory usage is 558100 kilobytes
138
139 Writing NGD file "top.ngd" ...
140 Total REAL time to NGDBUILD completion: 55 sec
141 Total CPU time to NGDBUILD completion: 27 sec
142
143 Writing NGDBUILD log file "top.bld"...
144
```

**Figure 8: Partition Implementation Status in Report Files**

The three team member partitions are all listed as Black Box Module. Partition information is provided in every report file (NGDBuild, Map, and PAR). This allows you to easily verify the status of all partitions on a given run.

## Step 4: Promoting Synthesis and Creating Team Member Projects

The design is now ready for the team members to start their work.

- Before generating PlanAhead projects for each team member, promote the initial *synthesis* results.
- Because the *implementation* results of the previous step are not used by team members, the *implementation* results need not be promoted.

### Promoting Successful Synthesis Results

To promote the successful synthesis results after synthesis (or implementation) has completed:

1. Click **Promote Partition** in the Flow Navigator (located under Implementation).
2. In the Promote Partitions dialog box, select only the Top partition to be promoted in the **synth\_1** run.

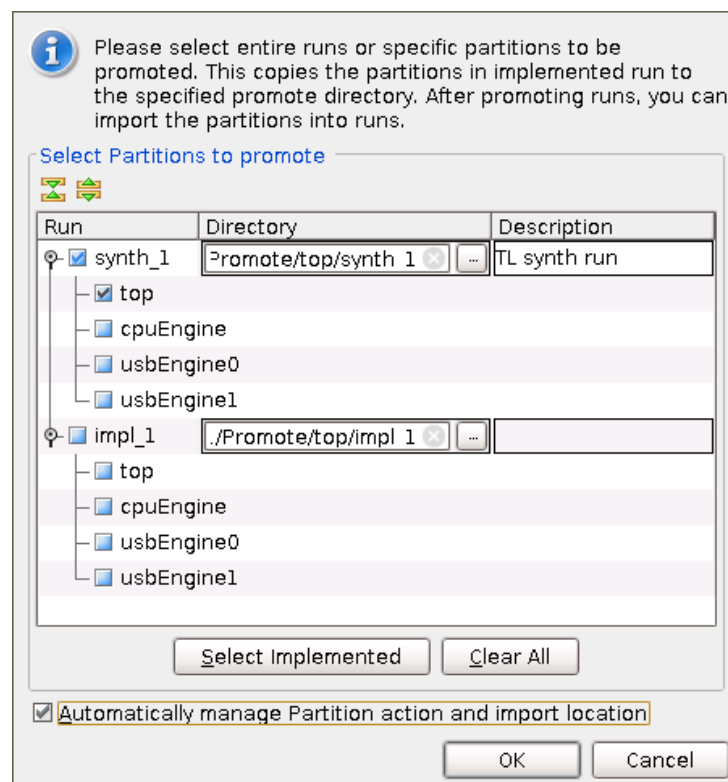


Figure 9: Promote Partitions Dialog Box

Do not to promote other partitions at this stage. No useful data exists for the other partitions. Promoting them will require additional steps by each team member to change the promoted partition state values back to implement for their runs.

3. Set the Promote directory for **synth\_1** to:

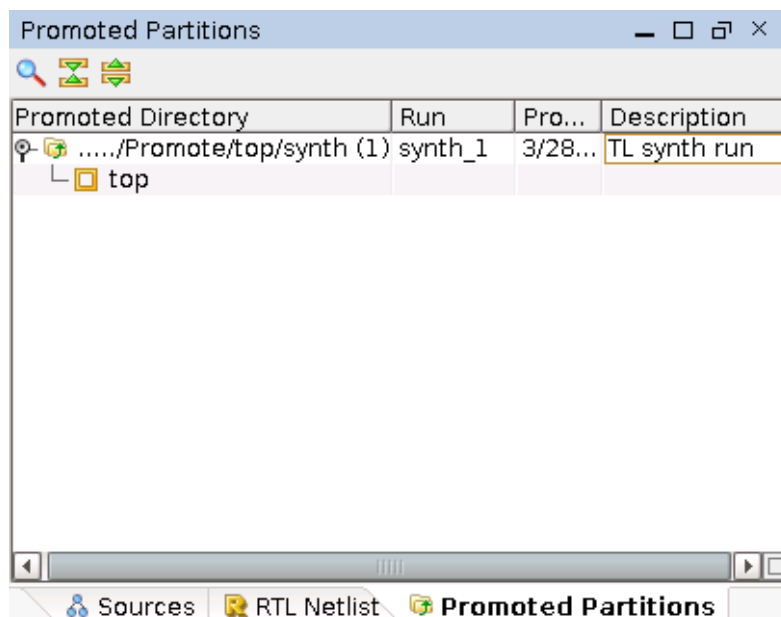
<Extract\_Dir>/Promote/top/synth\_1

The default Promote location could be used, but since this promoted data will be accessed by multiple team members it may be desirable to Promote this to a location external to the project directory.

4. Enter an optional description about the promoted data.
5. Verify that **Automatically Manage Partition Action and Import Location** is checked.  
 Checking **Automatically Manage Partition Action and Import Location** enables the PlanAhead tool to update the partition state and import location for the next synthesis run, whether by the team leader or by a team member. If this box is not checked, the team leader must manage these attributes.
6. Click **OK** to promote the Top partition synthesis results.
7. View the changes caused by promoting partitions. See the figure below (*Promoted Partitions Window*).
8. A Promoted Partitions tab now appears in the Elaborated Design view.

If you do not see this tab, select **Window > Promoted Partitions**.

The Specify Partitions dialog box now shows that the Action on the Top partition is Import. To open the Specify Partitions dialog box, click the **Specify Partitions** button in the Flow Navigator.



**Figure 10: Promoted Partitions**

## Creating Team Member Projects for usbEngine and cpuEngine

To create a consistent starting point for all team members, create multiple copies of the initial project. For this tutorial, you will create:

- One project for the **cpuEngine** instance
- One project for the two **usbEngine** instances.

These instances are the same module and are managed by a single team member.

To create team member projects for **usbEngine** and **cpuEngine**:

1. Select **File > Save Project As**.
2. Enter **project\_TM\_usbEngine** as the Project Name
3. Verify **Create Project Subdirectory** is checked.
4. Specify the following as the Project location:  
`<Extract_Dir>/Tutorial_Created_Data`
5. Click **OK**.
6. Repeat the above steps with the following parameters:
  - Project Name  
**project\_TM\_cpuEngine**
  - Project location  
`<Extract_Dir>/Tutorial_Created_Data`

---

## Step 5: Working on cpuEngine as Team Member

Acting as the team leader in the previous steps, you have:

- Set up the design.
- Created a workspace for each team member.

You will now switch roles and implement each block as a team member.

While the work of the team members is usually done in parallel, for this tutorial each team member block is handled sequentially.

For each team member project, you will:

- Update the project sources to include the completed logic for the team member block.
- Synthesize the project.
- Implement the project.
- Promote the results.

### Adding Sources to cpuEngine

Begin by adding sources to the **cpuEngine** project since it is already open from the last step. Make sure that the current PlanAhead project is **project\_TM\_cpuEngine**. If it is not, open this project now.

To add sources to **cpuEngine**:

1. Switch to the Project Manager view by click on Project Manager in the Flow Navigator.
2. In the Sources window, use the Hierarchy tab to expand top and select cpuEngine (or1200\_bb.v).

This is the black box module for **cpuEngine** that was used for the initial project. You will now replace this black box module with logic.

3. Right-click, and select **Remove from Project**.
4. Click **OK**.

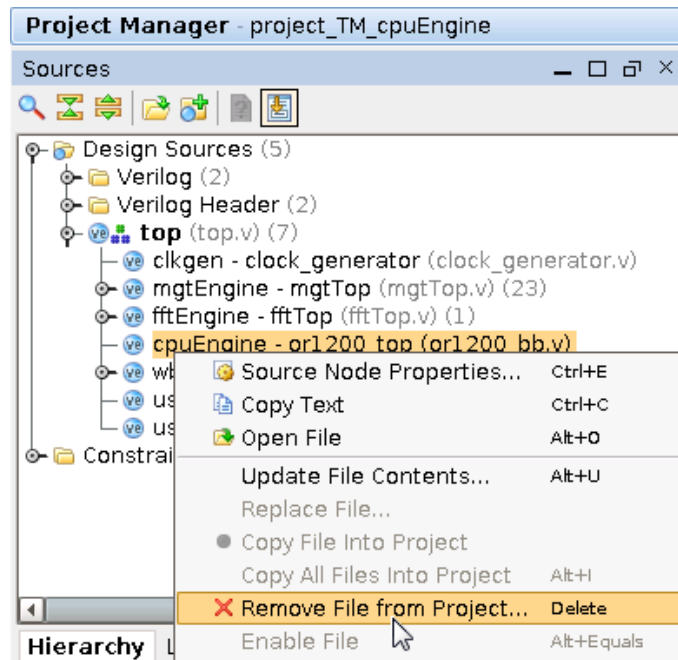

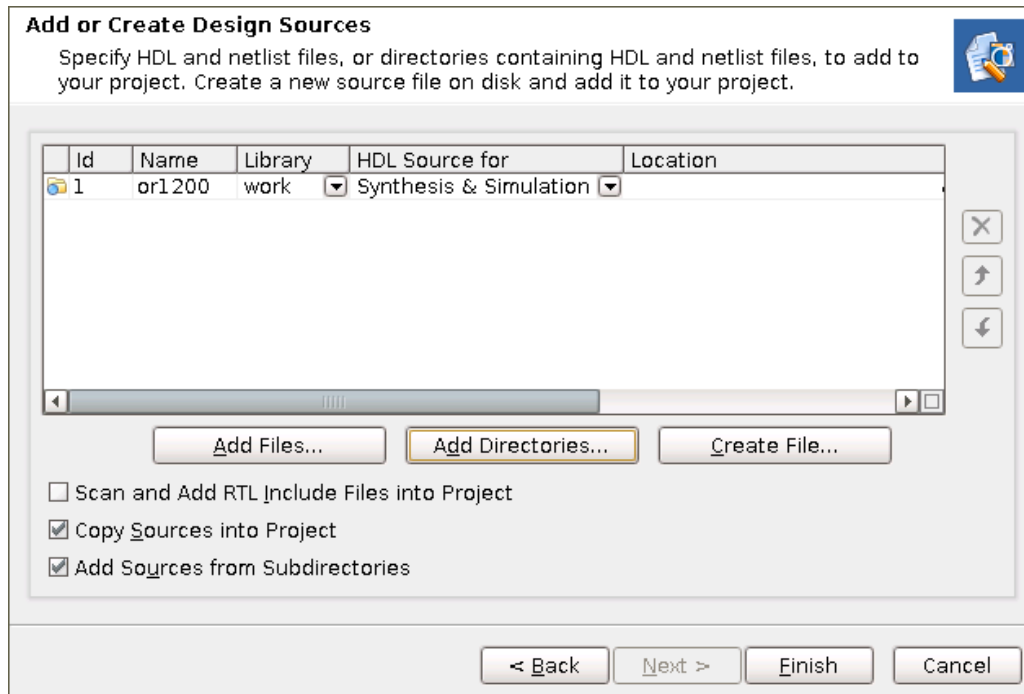


Figure 11: Remove or1200\_bb.v Black Box Module

5. At the top of the Sources window, click the **Add Sources** icon (  ).
6. From the Add Sources wizard, select **Add or Create Design Sources**.
7. Click **Next**.
8. Click **Add Directories** to add the completed sources for the **cpuEngine** instance.
9. Browse to the following location:
 

```
./Sources/hdl/.
```
10. Select the or1200 directory.

11. Click **Select**.



**Figure 12: Add Source Directory or1200**

12. Verify the directory to be added.

13. Click **Finish**.

14. You should now see the cpuEngine module can be expanded in the Hierarchy sources view.

## Synthesizing and Implementing cpuEngine

The Elaborated Design and Synthesized Design views are now out of date. To update them, you will:

- Reload (or close and reopen) these views.
- Verify the partition settings for synthesis and implementation.
- Launch the runs.
- Promote the results.

To reload the design:

- 1 If the Elaborated Design view was closed, click **Open Elaborated Design** in the Flow Navigator to load the latest version of the design.

- If the Elaborated Design view is open, the banner across the top states that the view is out of date. Click **Reload** to reload the view.



Figure 13: Banner with Elaborated Design Status

- Verify that **cpuEngine** is no longer a black box, and note that the two usbEngine instances will remain a black box for this project.
- Click **OK**.
- In the Flow Navigator, click **Specify Partitions** (located under Project Manager).  
In the Specify Partitions dialog box, verify the partition settings for synthesis and implementation.

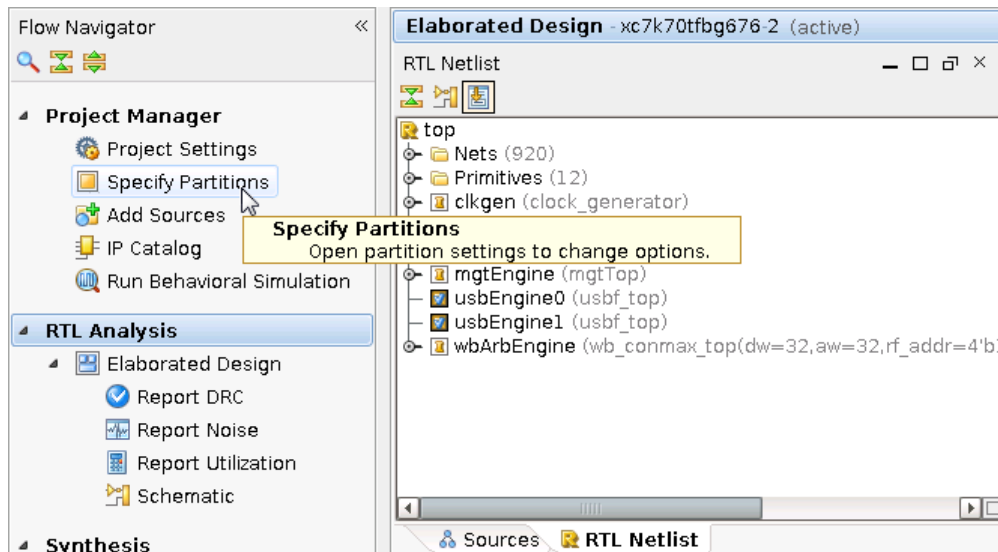


Figure 14: Specify Partitions

- From the Synthesis tab, verify that:
  - Top is set to **Import**.
  - All other partitions are set to **Implement**.

There is no other data to import besides the top-level synthesis results. Top is the only partition that has been promoted.



If Top is not set to *import* for synthesis, either of the following might have occurred:

- Top was not promoted correctly.
- Automatically Manage Partition Action and Import Location was not checked in the Promote Partition dialog box.

If Top was not correctly promoted, it cannot be imported now.

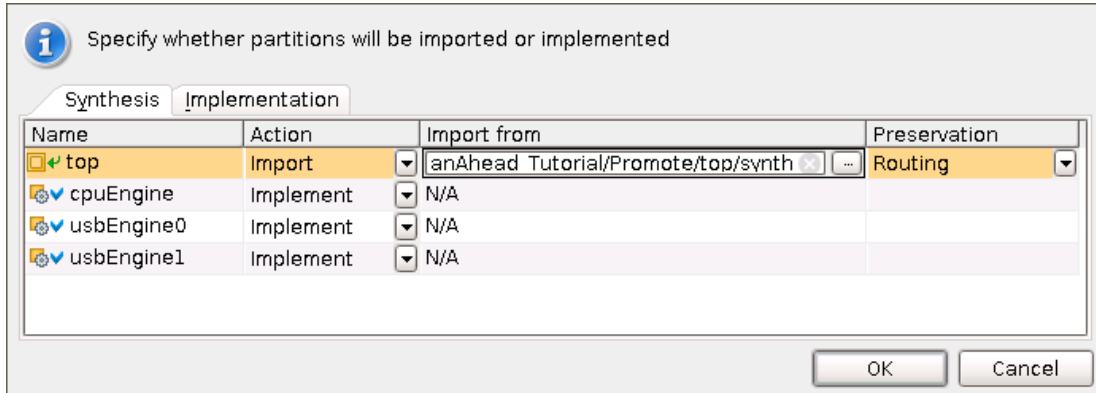


Figure 15: Specify Partitions Dialog Box

8. Click the **Implementation** tab to verify that all partitions are set to **Implement**.
9. Click **OK**.

### Optional Steps

You can skip the next two steps to save time. Instead of running synthesis and implementation, open the completed project at:

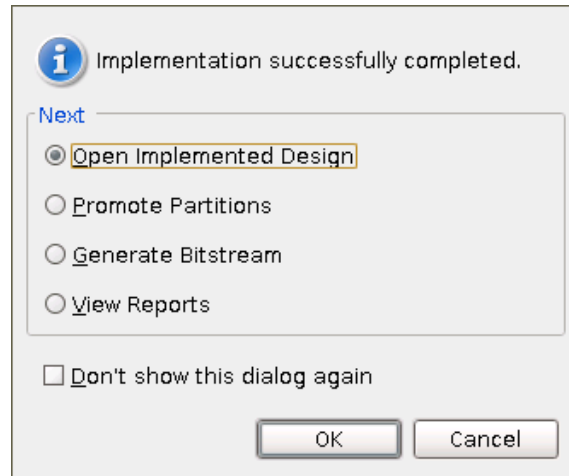
`<Extract_Dir>/Projects/project_TM_cpuEngine_completed`

1. In the Flow Navigator, click **Run Implementation** to synthesize and implement the design.  
A message reports that synthesis is out-of-date.
2. Click **Yes** to launch synthesis prior to implementation.

### Verifying and Promoting Results of cpuEngine

If you ran synthesis and implementation, the Implementation Completed dialog box displays when implementation completes.

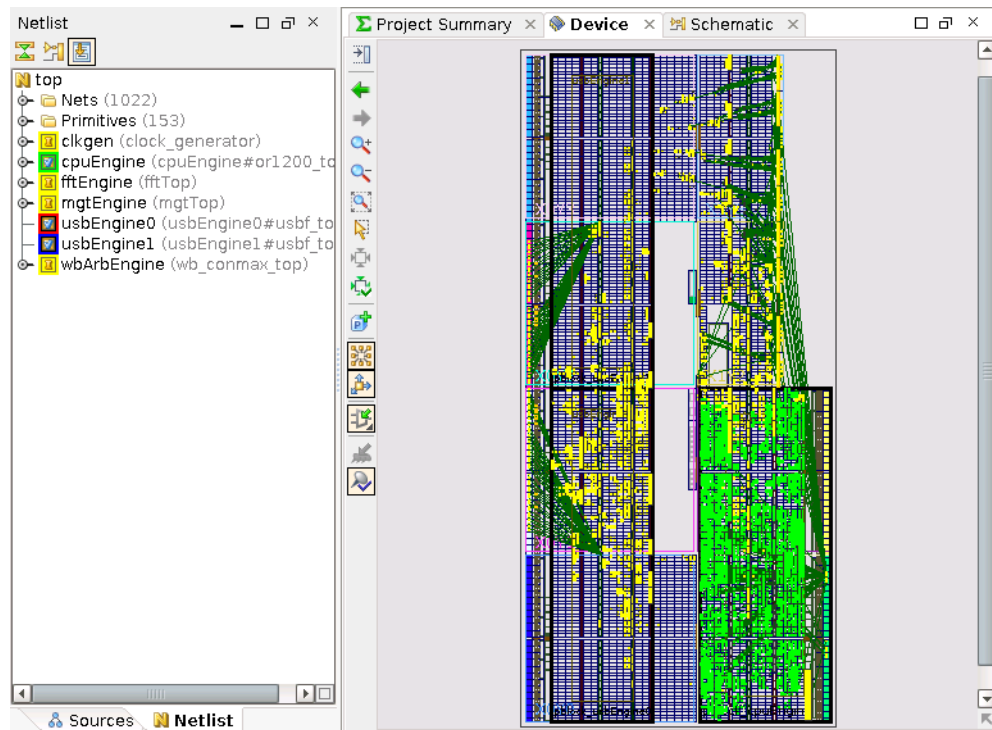
1. In the Implementation Completed dialog box, select **Open Implemented Design**.
2. Click **OK**.



**Figure 16: Specify Partitions Dialog Box**

If you skipped running implementation and opened the **project\_TM\_cpuEngine\_completed** design, or if the Implementation Completed dialog box did not open:

3. In the Flow Navigator, click **Open Implemented Design**.
  - The Implemented Design view shows that:
    - The Pblock for **cpuEngine** is relatively full.
    - The Pblocks for the two **usbEngine** instances are relatively empty.
  - Because the **usbEngine** instances were black boxes, no logic exists for these two blocks in the implemented design.
  - The logic belonging to the Top partition is highlighted in yellow in the following figure (*Implemented Design View of the cpuEngine Project*).
    - This logic appears in the **usbEngine** Pblocks because it was not restricted from being placed inside these Pblocks.



**Figure 17: Implemented Design View of the cpuEngine Project**

The Highlight Primitives tool can be used to create a highlighted view as shown in the figure above (*Implemented Design View of the cpuEngine Project*).

4. To verify that timing has been met, review any of the following:
  - The Timing Score in the Design Runs view
  - The details of the Timing Results window
  - The Timing Score in the Project Summary window
5. In the Flow Navigator, click **Promote Partitions** to promote the successful synthesis and implementation results.

If the Elaborated Design view is not opened, you are prompted to open it. Click **OK**.

6. Select only the **cpuEngine** instance in both the synthesis and implementation runs.
7. Set the Promote directories.
  - synth\_1: <Extract\_Dir>/Promote/cpuEngine/synth\_1
  - impl\_1: <Extract\_Dir>/Promote/cpuEngine/impl\_1

The Promote directory used in team design should be a network location or repository that is accessible by all team members. This tutorial changes the default promote location to a folder outside the project directory structure to emulate such a location.

8. Uncheck **Automatically Manage Partition Action and Import Location**.

While disabling **Automatically Manage Partition Action and Import Location** is not critical to this tutorial, Xilinx recommends removing it for team members in a team design flow.

The **cpuEngine** team member might continue working on this block. Removing this option prevents the software from automatically importing **cpuEngine** on the next run.

These promoted results are imported by the team leader in a later step, but are not imported by the team member who is promoting it.

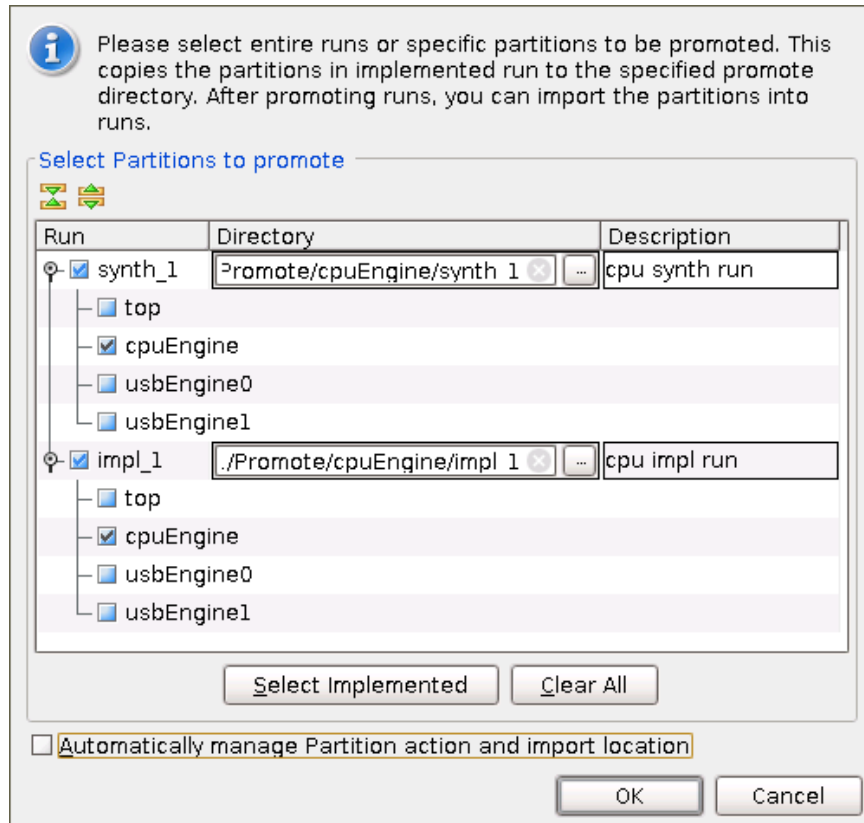


Figure 18: Promote Settings for cpuEngine

9. Click **OK**.

---

## Step 6: Working on usbEngine as Team Member

In this Step, you will repeat the procedures of Step 5 as a team member working on **usbEngine**.

If multiple processors are available, you can perform this step in parallel while the **cpuEngine** project is implementing.

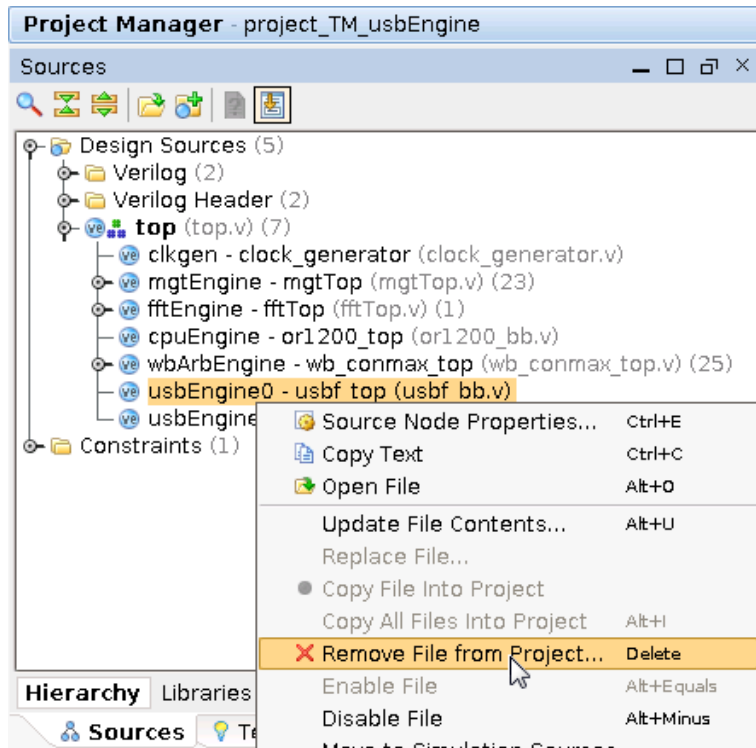
### Adding Sources to usbEngine

To add sources to **usbEngine**:

1. Close the current open project unless:
  - You are doing this step in parallel, and
  - The **cpuEngine** has not yet finished implementation, or has not been promoted.
2. Open the PlanAhead project:  
`<Extract_Dir>/Tutorial_Created_Data/project_TM_usbEngine`
3. Click the **Project Manager** view.
4. In the Sources window, use the Hierarchy tab to expand top and select one of the two usbEngine instances (`usbfb_bbb.v`).  

This black box module definition is used for the two **usbEngine** instances in the initial project. It will now be replaced with logic.
5. Right-click.
6. Select **Remove from Project**.

7. Click **OK**.



**Figure 19: Remove Black Box Module usbf\_bb.v**

8. At the top of the Sources window, click the **Add Sources** icon ( ).
9. From the Add Sources wizard, select **Add or Create Design Sources**.
10. Select **Next**.
11. Click **Add Directories**.
12. Browse to:
  - /Sources/hdl/
13. Select the `usbf` directory to add the completed sources for the **usbEngine** instance.
14. Click **Select**.
15. Click **Add Files**
16. Select the file:
  - /Sources/hdl/rtlRam.v
17. Verify the file and directory to be added.
18. Click **Finish**.

## Synthesizing and Implementing usbEngine

To synthesize and implement **usbEngine**:

1. In the Flow Navigator, click **Open Elaborated Design** to open the Elaborated Design view.
2. Verify that the two **usbEngine** instances are no longer black boxes.
3. In the Flow Navigator, click **Specify Partitions** (located under Project Manager).
5. From the Synthesis tab, verify that:
  - Top is set to **Import**.
  - All other partitions are set to **Implement**.

There is no other data to import besides the top-level synthesis results. Top is the only partition that has been promoted.

If Top is not set to *import* for synthesis, either of the following might have occurred:

- Top was not promoted correctly.
- Automatically Manage Partition Action and Import Location was not checked in the Promote Partition dialog box.

If Top was not correctly promoted, it cannot be imported now.

6. Click the **Implementation** tab to verify that all partitions are set to **Implement**.
7. Click **OK** to exit the Specify Partitions dialog box.

### Optional Steps

You can skip the next two steps to save time. Instead of running synthesis and implementation, open the completed project at:

```
<Extract_Dir>/Projects/project_TM_usbEngine_completed
```

1. In the Flow Navigator, click **Run Implementation** to synthesize and implement the design.  
A message reports that synthesis is out-of-date.
2. Click **Yes** to launch synthesis prior to implementation.

## Verifying and Promoting Results of usbEngine

To verify and promote results of **usbEngine**:

1. Open the Implemented Design view.  
If you ran synthesis and implementation, the Implementation Completed dialog box displays when implementation completes.
2. In the Implementation Completed dialog box, select **Open Implemented Design**.

3. Click **OK**.

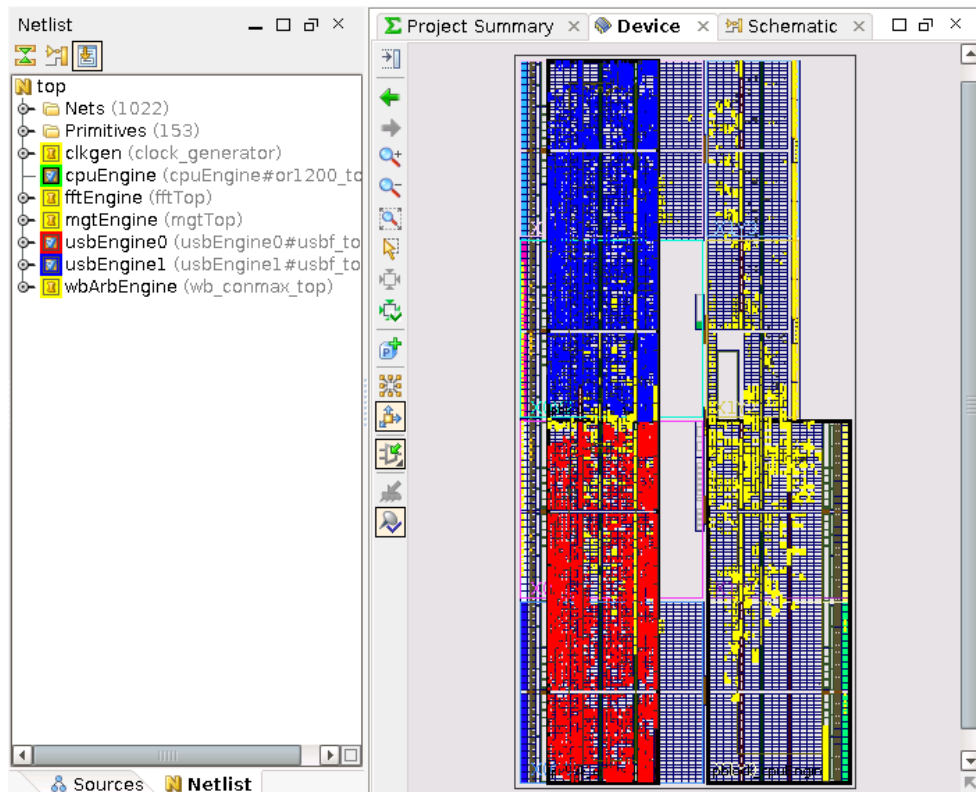
If you skipped running implementation and opened the **project\_TM\_usbEngine\_completed** design, or if the Implementation Completed dialog box did not open, click **Open Implemented Design** from the Flow Navigator.

4. The Implemented Design view shows that:

- The Pblocks for **usbEngine0** and **usbEngine1** are relatively full.
- The Pblock for the **cpuEngine** instance is relatively empty.

Because the **cpuEngine** instance was a black box, it is expected to be empty. However, some logic can be seen in this region. The logic from the top level partition was not restricted from being placed inside the **cpuEngine** Pblock.

You can use the Highlight Primitives tool to create a highlighted view.



**Figure 20: Implemented Design View of the usbEngine Project**

5. To verify that timing has been met, review any of the following:

- The Timing Score in the Design Runs view
- The details of the Timing Results window
- The Timing Score in the Project Summary window



6. In the Flow Navigator, click **Promote Partitions** to promote the successful synthesis and implementation results.
7. If the Elaborated Design view is not opened, you are prompted to open it. Click **OK**.
8. Select only the **usbEngine0** and **usbEngine1** instances in both the synthesis and implementation runs.
9. Set the Promote directories.
  - synth\_1: <Extract\_Dir>/Promote/usbEngine/synth\_1
  - impl\_1: <Extract\_Dir>/Promote/usbEngine/impl\_1
10. Uncheck **Automatically Manage Partition Action and Import Location**.

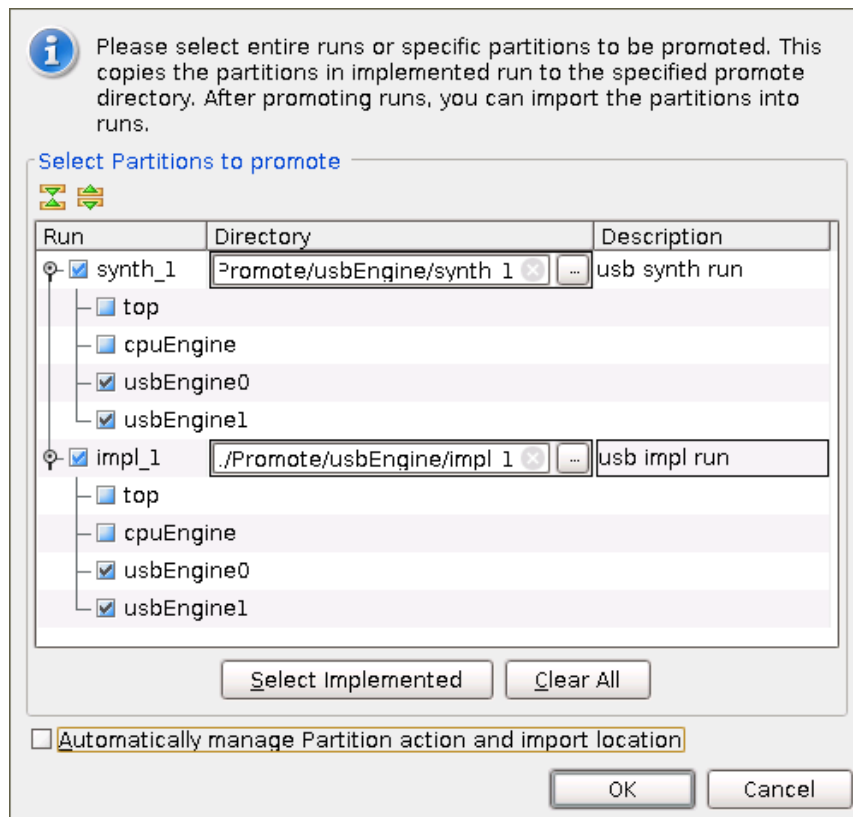


Figure 21: Promote Settings for usbEngine0 and usbEngine1

11. Click **OK** to promote the **usbEngine0** and **usbEngine1** partitions.

---

## Step 7: Running the Assembly as Team Leader

In the previous steps, each team member synthesized, implemented, and promoted a version of their block. The team leader can now assemble the design. The team leader:

- Reopens the team leader project.
- Sets up the partitions for import.

### Setting Up the Team Leader Project To Do an Assembly Run

To set up the team leader project to do an assembly run:

1. Reopen the following project:

`<Extract_Dir>/Projects/project_TL`

This is the original project. It already contains:

- The defined team member partitions
  - The successful synthesis results of Top
  - The Pblocks for the team member blocks
2. Update the project to define the team member blocks as logic instead of black boxes. To do this, add the successful synthesis results (NGC) from each team member's promoted synthesis run.
  3. From the Project Manager, click **Add Sources**.
  4. Select **Add or Create Design Sources**.
  5. Click **Next**.
  6. Select **Add Files**.
  7. Add the following files:
    - `<Extract_Dir>/Promote/usbEngine/synth_1/usbEngine0#usbf_top.ngc`
    - `<Extract_Dir>/Promote/usbEngine/synth_1/usbEngine1#usbf_top.ngc`
    - `<Extract_Dir>/Promote/cpuEngine/synth_1/cpuEngine#or1200_top.ngc`
  8. Click **Finish**.

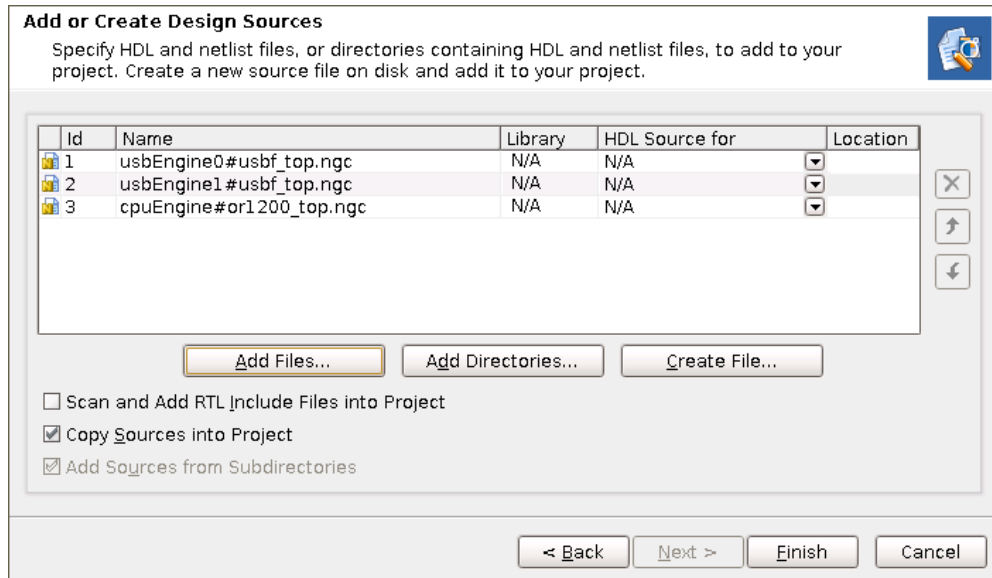


Figure 22: Add Post Synthesis Results for Team Member Partitions

- In the Flow Navigator, click **Open Synthesized Design** to open the Synthesized Design view. All partitions are now defined for this project. It is not necessary to rerun synthesis. The latest synthesis results of all team members (including the team leader) are used for this assembly run.

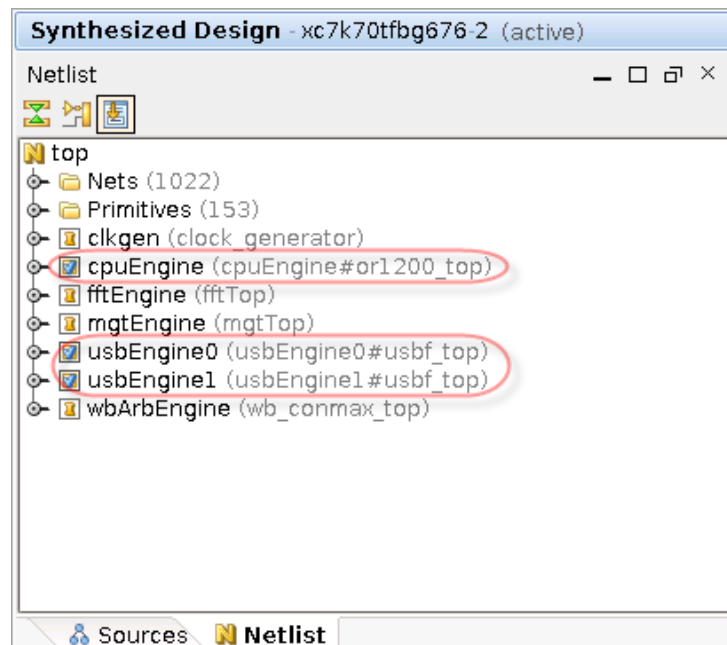


Figure 23: Synthesized Design With All Partitions Defined, and No Black Boxes

## Updating Partition Settings and Running the Assembly

To update partition settings and run the assembly:

1. In the Flow Navigator, click **Specify Partitions** and access the **Implementation** Partition settings. The Synthesis tab can be left as is since synthesis is not being ran.
2. Leave the Top partition action as **Implement**.
3. Change the following remaining partition actions to **Import**:
  - cpuEngine
  - usbEngine0
  - usbEngine1
4. Change the **Import from** field to the location to which the team members promoted the implementation results.
  - cpuEngine: <Extract\_Dir>/Promote/cpuEngine/impl\_1
  - usbEngine0: <Extract\_Dir>/Promote/usbEngine/impl\_1
  - usbEngine1: <Extract\_Dir>/Promote/usbEngine/impl\_1

Because both **usbEngine** instances were implemented together and promoted together, the **Import From** location is also the same.

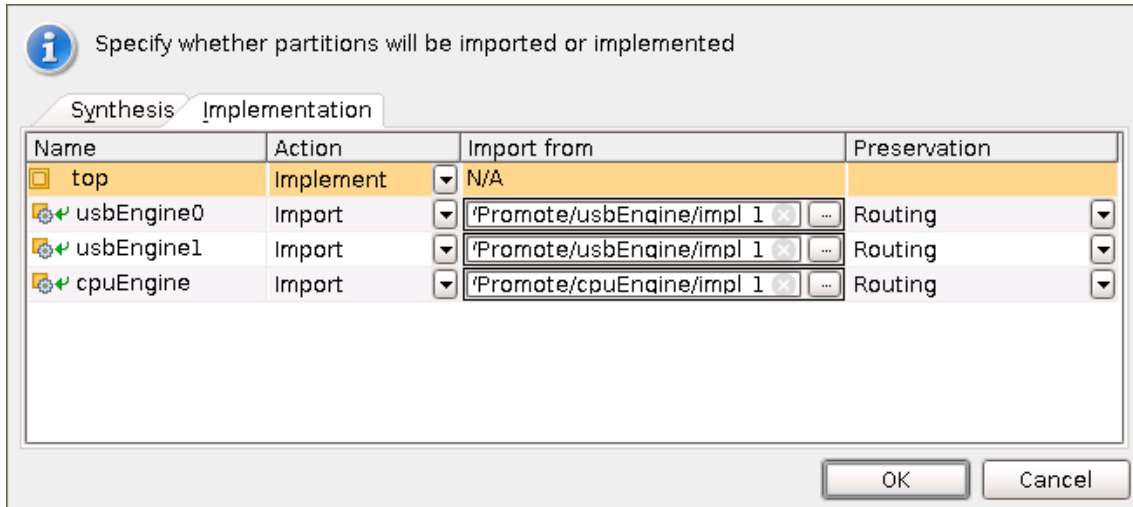


Figure 24: Partition Settings for Assembly Run

5. Click **OK**.
6. Click **OK** on the Reset out-of-date run dialog to reset **impl\_1**.

You do not need to run the next step in which you run implementation. To save time, open the completed project at:

<Extract\_Dir>/Projects/project\_TL\_assembled

- Optional. Click **Run Implementation** in the Flow Navigator to launch implementation and assemble the full design.

## Verifying and Promoting Assembly Results

In this design:

- Each team member block is logically isolated from other team member blocks.
- All the boundaries are registered.
- The placement of each team member block was sufficient the first time through.

For more complex designs, this assembly run may be the first of many. The process described in this tutorial may be repeated as necessary.

Each team member project can now start to import other team member blocks from this promoted assembly run. This helps interface timing to converge early in the design cycle, instead of leaving other team member blocks as black boxes and discovering interface timing issues at the end of the design.

To verify and promote the assembly results:

- Open the Implemented Design view.
- In the Implementation Completed dialog box, select **Open Implemented Design**.
- Click **OK**.

If you skipped running implementation and opened `project_TL_assembled`, or if the Implementation Completed dialog box did not open, click **Open Implemented Design** from the Flow Navigator.

When the Implemented Design view opens, you can see the entire design. The figure below (*Implemented Design View of the Assembled Design*) shows an example of this placement. The figure uses the highlight colors shown in the following table.

Item	Highlight Colors
usbEngine0	red
usbEngine1	blue
logic belonging to the Top partition	yellow
cpuEngine	green

You can use the Highlight Primitives tool to create this highlighted view.

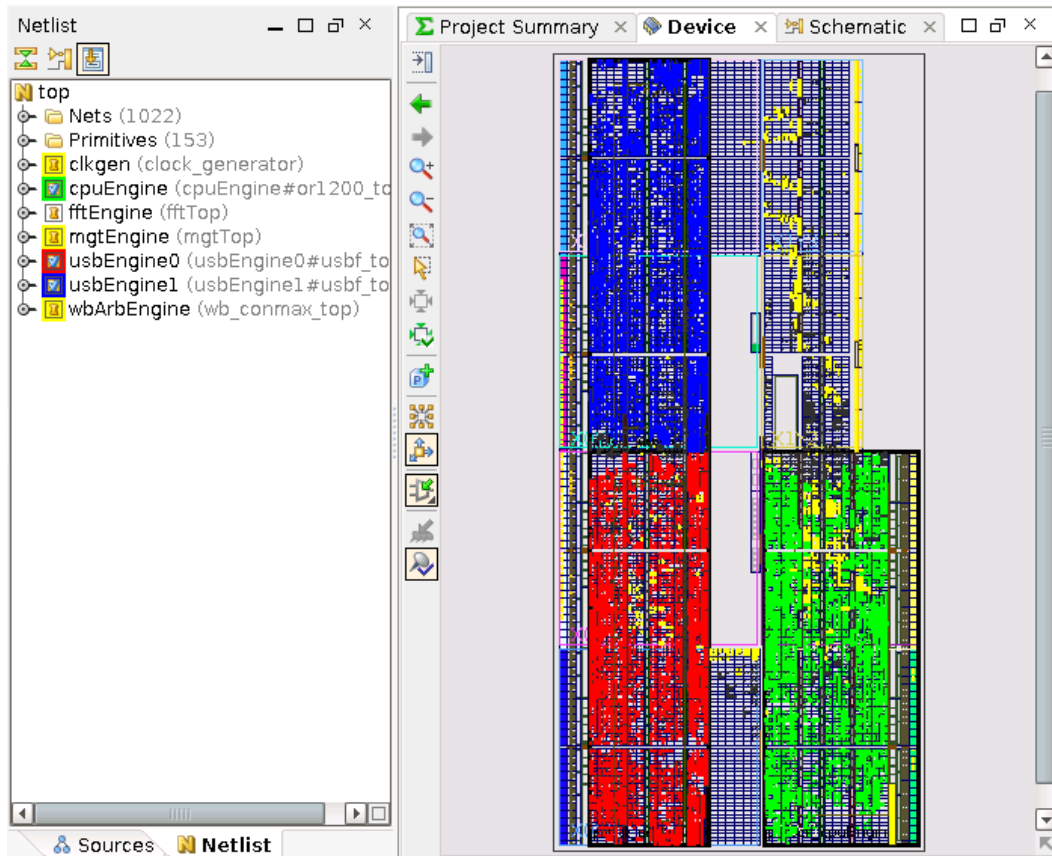


Figure 25: Implemented Design View of the Assembled Design

## Verifying That Timing Has Been Met

To verify that timing has been met, review any of the following:

- The Timing Score in the Design Runs view
- The details of the Timing Results window
- The Timing Score in the Project Summary window

## Verifying That All Team Member Partitions Were Imported

To verify that all team member partitions were imported, review the Implemented Partition section of the Project Summary view.

Implemented Partitions			
<b>top</b>		<b>cpuEngine</b>	
Type:	Normal	Type:	Normal
State:	Implement	State:	Import
PAR Preservation Level:	Routing	Import Location:	ote/cpuEngine/impl
Boundary Optimization:	None	PAR Preservation Level:	Placement
		Modified Import Logic:	Routing
		Boundary Optimization:	None
<b>usbEngine0</b>		<b>usbEngine1</b>	
Type:	Normal	Type:	Normal
State:	Import	State:	Import
Import Location:	ote/usbEngine/impl	Import Location:	ote/usbEngine/impl
PAR Preservation Level:	Placement	PAR Preservation Level:	Placement
Modified Import Logic:	Routing	Modified Import Logic:	Routing
Boundary Optimization:	None	Boundary Optimization:	None
Go To: <a href="#">Specify Partitions</a>			

Figure 26: Partition Summary Section of Project Summary

## Promoting Successful Synthesis and Implementation Results

Modifications to the design may require some or all of this flow to be repeated. Using these successful assembly results in future iterations may be beneficial. To promote the successful synthesis and implementation results:

1. In the Flow Navigator, click **Promote Partitions**.
2. If the Elaborated Design view is not opened, you are prompted to open it. Click **OK**.
3. Select all partitions in both the synthesis and implementation to be promoted.

Because the placement of the Top partition meets all interface timing, each team member can now begin to import Top, as well as other team member partitions to maintain this interface timing in all future iterations.

4. Set the Promote directories:
  - synth\_1: <Extract\_Dir>/Promote/top/synth\_1
  - impl\_1: <Extract\_Dir>/Promote/top/impl\_1

For this tutorial, the synthesis results for the team leader have not changed from the last time they were promoted. However, the team leader might develop additional logic in the top level design in parallel with the other team members. In this case, promoting synthesis

and implementation results at this stage ensures that all team members are working on the latest code.

5. Uncheck **Automatically Manage Partition Action and Import Location**.

Disabling **Automatically Manage Partition Action and Import Location** prevents the software from automatically changing the import locations of the team member partitions to the location to which they were just promoted (`Promote/top`).

Instead, the software maintains the locations defined in the previous steps. This simplifies running the assembly step in future iterations.

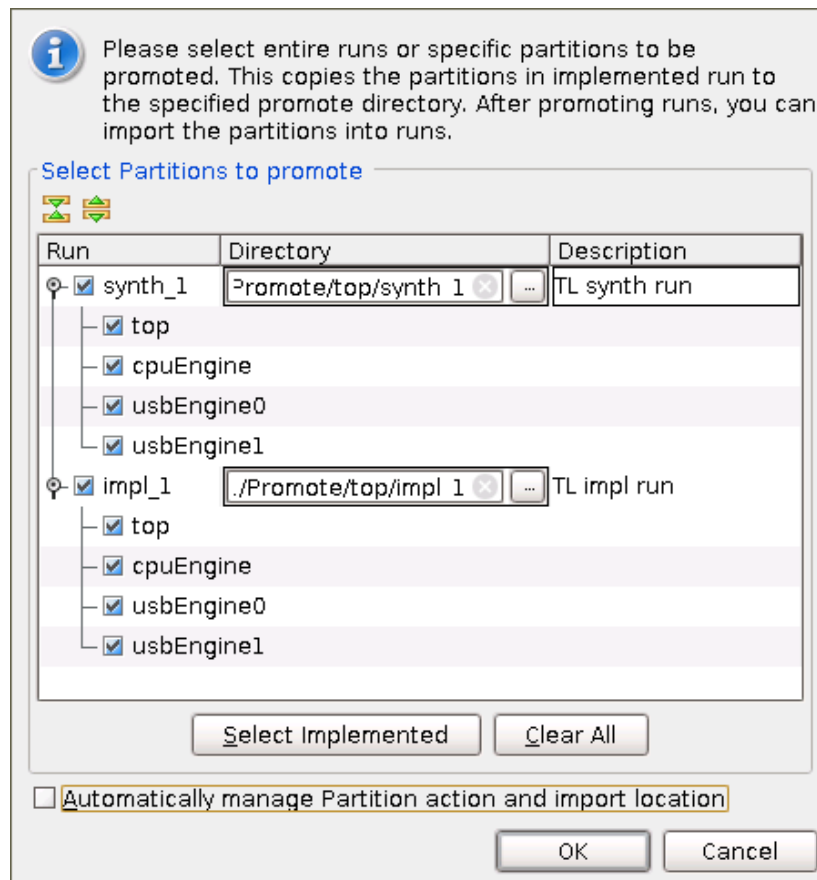


Figure 27: Promote Settings for Assembled Design

6. Click **OK**.



---

## Conclusion

In this tutorial, you did the following:

- Used partitions and the Team Design methodology to synthesize and implement a design in multiple parts.
- Assembled the full design.
- Synthesized and implemented blocks as black boxes.
- Promoted successfully synthesized and implemented partitions to a central repository.
- Created PlanAhead projects for each team member.