Registration Form for Three Day Workshop on
"VLSI and Embedded System Design"
(VESD-2017, October 13-15, 2017)
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Name:_____
Affiliation:_____
Department:_____
Specialization_____
Address:_____
State:_____Postal Code:_____
E-mail ID:_____
Mobile Number:_____
Registration Type (Please Underline):
UG & PG / PhD Students / Faculty / Industry
Registration Fee (Rs.)*: 250 / 500 / 750 / 1500
Do you want accommodation?: Yes / No
Gender: Male / Female

Payment Details

Registration Fee:
DD/Cheque/Transaction Number:
(Fee Payment: *in favour of* **CEP IIT Bhubaneswar)**
Date of Payment:
Branch Name:
*Registration Fee includes Registration kit and Tea/Snacks (Not including accommodation)

Embedded System Expo

Do you want to demonstrate your project?: Yes / No
Tile of the Project:_____
_____

Signature:_____

Please send a copy of registration form along with payment detail to the email ID:
msm@iitbbs.ac.in

Online Registration (Please Click)

https://docs.google.com/forms/d/e/1FAIpQLSeF_LpNlZ8HP9B97H1mPMLB5578DIsfsl4jQCievqz1MHku0Q/viewform

Last Date for Registration: 09 October 2017

Embedded System Expo Awards

1st Prize (02): 2500; 2nd Prize (02): 1500

Who Can Participate?

- Faculty/Technical Staff/Research Scholars with area of interests of VLSI Design and Embedded Systems
- UG/PG Students who require hands-on training on embedded system design projects

A THREE DAY WORKSHOP ON
VLSI and Embedded System Design (VESD-2017)

|October 13-15, 2017 | IIT Bhubaneswar| Odisha-752050 |

About the Workshop

The Real-time Embedded System Laboratory at the School of Electrical Sciences, Indian Institute of Technology Bhubaneswar will organize "A Three Day Workshop on "**VLSI and Embedded System Design**" from 13th October to 15th October 2017 in association with CoreEL Technologies (I) Pvt Ltd, Bangalore. This workshop is a combination of lecture and hands-on practice on VLSI and Embedded based System Design tools for providing innovative system design aspects by addressing the key developmental challenges of Wearable Devices, Internet of Things (IoT), and Automation System. A special session on "**Embedded System Expo**" is also being organized to offer a great opportunity for displaying the design projects with presentations by the participants. Three Awards will be given for the best embedded system projects.

Workshop Focus

- VLSI Design Flow and CAD Tools [Xilinx Vivado Tool, Mentor Graphics HDL Designer]
- VHDL Synthesis and Verification
- IP Integrator and Embedded System Design Flow
- FPGA Based Design using Xilinx System Generator
- Embedded System Design for Wearable Devices
- Opportunities & Challenges in Implementing IoT Solutions
- Arduino Based Monitoring System Design (Audio, Biomedical, Power Quality, Environmental Condition)

Programme Coordinators

- Dr. M. Sabarimalai Manikandan, IIT Bhubaneswar
- Dushyant Gupta, Associate Manager, CoreEL
- G. Prakash, Technical Support Specialist, CoreEL
- Dr. Barathram.Ramkumar, IIT Bhubaneswar
- Dr. Srinivas Bhaskar Karanki, IIT Bhubaneswar

Outcomes of this Workshop

- Hands-on experience on VLSI design tools
- Create and debug HDL designs
- Hands-on experience on FPGA based design
- Hands-on experience on Arduino based monitoring projects
- Participation certificate

Please contact for any queries:

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Three Day Workshop on "VLSI and Embedded System Design (VESD-2017)"

Workshop Content

Day 1 (13 October 2017)

- VLSI Design Technology Trends and CAD Tools
- 7-Series Architecture Overview
- Vivado Design Flow
- **Lab 1: Creating an HDL Design**
  - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bit stream and debug the design using Vivado Logic Analyzer
  - IP Integrator and Embedded System Design Flow
- **Lab 2: Create a Processor System using IP Integrator**
  - Create a simple ARM Cortex-A9 based processor design targeting the Zed Board using IP Integrator.
- **Lab 3: Debugging using Vivado Logic Analyzer cores**
  - Insert various Vivado Logic Analyzer cores to debug/analyze system behavior.

Day 2 (14 October 2017)

- Embedded System Design with Custom IP
- **Lab 4: Creating and Adding Your Own Custom IP**
  - Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral. Write a basic C application to access the peripherals.
  - System Debugging using Vivado Logic Analyzer and SDK
- **Lab 5: Debugging using Vivado Logic Analyzer cores**
  - Insert various Vivado Logic Analyzer cores to debug/analyze system behavior.
  - Profiling and Performance Improvement
  - Introduction to High-Level Synthesis with Vivado HLS
  - Improving Performance and Resource Utilization
  - Creating an Accelerator
- **Lab 6: Creating a Processor System using Accelerator**
  - Profile an application performing a function both in software and hardware.
  - Create an accelerator in Vivado HLS.
  - Use the generated accelerator to build a complete system

Day 3 (15 October 2017)

- **Fundamentals of VLSI chip design methodology**
  - Basics of ASIC & FPGA
  - Concepts of HDL design and verification for front end
  - Synthesis technique overview w.r.t. ASIC & FPGA
  - Details of ASIC foundry & technology
  - Concepts of DFT and DFT verification
- **Lab on HDL Design flow for front end**
  - HDL design, verification & synthesis
  - Understanding netlists for ASIC & FPGA
  - Hands on Session
- **Concepts of ASIC Full custom & Semi-custom methodologies**
  - Understanding Back end design with Layout design flow
  - Concepts of SDL & RTL to GDSII
  - Calculating Area, Timing & Power & optimizing
  - Layout verification methodologies (DRC,LVS,PEX,DFM,PERC)
  - Post-layout verification or Back annotation & exporting to GDSII
  - Concepts of DFT