COURSE HIGHLIGHTS

- Use Xilinx Design Constraints to communicate performance
- Rapidly architect an embedded system targeting the ARM processor of Zynq Device using Vivado and IP Integrator
- Extend the hardware system with Xilinx provided peripherals
- Create a custom peripheral and add it to the system
- Debug a design using Vivado hardware analyzer
- Use Vivado HLS to generate an IP-XACT compliant hardware accelerator.

COURSE CONTENT

Day 1:

- 7-Series Architecture Overview
- Vivado Design Flow
- **Lab 1: Creating an HDL Design (VIVADO)**
- **Lab 2: Xilinx Design Constraints**
- IP Integrator and Embedded System Design Flow
- **Lab 3: Create a Processor System using IP Integrator**

Day 2:

- Embedded System Design with Custom IP
- System Debugging using Vivado Logic Analyzer and SDK
- **Lab 4: Debugging using Vivado Logic Analyzer cores.**
- Profiling and Performance Improvement
- Introduction to High-Level Synthesis with Vivado HLS
- Improving Performance and Resource Utilization
- Creating an Accelerator
- **Lab 5: Creating a Processor System using Accelerator**
- **Lab 6: Real Time Video Processing Demo.**

ORGANIZING COMMITEE

Patron
Er.C.Marimuthu, Chairman.

Co-Patron
Dr.Aanat Achary, Principal.

Convenor
Dr.M.Sundaram, Prof & Head /ECE

Coordinators
Mr.J.Augustin Jacob, Asst.Professor / ECE
Mr.P.Aravind, Asst. Professor / ECE

RESOURCE PERSONS

Ms.Sadiya,
National Manager,
CoreEL Technologies, Bangalore.

Mr.G.Prakash,
Product Support Specialist,
CoreEL Technologies, Bangalore.

Mr.C.Siva Sathya Narayanan,
Territory Manager,
CoreEL Technologies, Bangalore.
Mail: upt@coreel.com
Cell No: 09843713132

For further enquries and communication,

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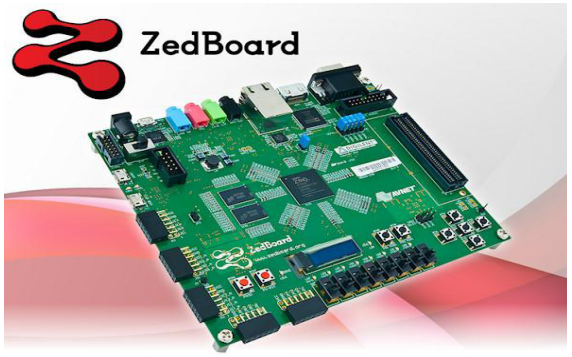
KAMARAJ
COLLEGE OF ENGINEERING & TECHNOLOGY
S.P.G.Chidambara Nadar - C. Nagammal Campus,
S.P.G.C.Nagar, VIRUDHUNAGAR.

Workshop on

System Design Using Vivado Design Suite and Zynq-7000 SoC

31st July & 1st August, 2015



Organized by
Department of Electronics and Communication Engineering

In Association with

CoreEL Technologies
Enabling Excellence

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ABOUT THE COLLEGE

Kamaraj College of Engineering and Technology is established in 1998-1999. It is rightly named after the son of the soil, Bharat Ratna Sri.K.Kamaraj who was the undisputed leader of the suppressed downtrodden and a champion of free education for Masses. Our College is approved by AICTE, New Delhi and affiliated to Anna University, Chennai. It is promoted and supported by Virudhunagar Hindu Nadar's Mahamai Tharappus in Virudhunagar. The college attracts outstanding students from different parts of Tamilnadu by virtue of its discipline and Infrastructure facilities.

ABOUT THE DEPARTMENT

The Department of Electronics and Communication Engineering is established in the year 1998. In 2011, the department started post graduate program, M.E. degree in Communication and Networking. The Department has 30 highly qualified and well experienced faculty members. It is well equipped with fully air conditioned laboratories in the areas of Microprocessors and Microcontrollers, VLSI, Digital Signal/Image Processing, Microwave and Optical Communication to cater the present academic and industry requirements. The Department is conducting various workshops and seminars to update students and faculty members with the knowledge of emerging fields towards industrial applications.

ABOUT CoreEL TECHNOLOGIES

CoreEL Technologies (I) Pvt Ltd, CoreEL is a customer Application Specific Products & Solutions company offering Intellectual Property (IP) Hardware, Software & Engineering Services to customers, enabling them to Design Manufacture and Market world class electronic products. The portfolio of offerings include IP cores, Sytem Design, Architecture, Validation, Sustenance, Prototype Manufacturing, Next-Gen products, Semiconductor solutions & Distribution of EDA Tools & COTS products. CoreEL was founded in 1999 and is an ISO 9001:2008 certified headquartered at Bangalore India.

ELIGIBILITY

Faculties from AICTE approved Engineering Colleges with relevant background. Candidates from industries and R & D organizations will also be considered. PG students in related discipline are also eligible.

PRE-REQUISITES

- Digital logic and FPGA design experience
- Basic experience with Verilog and VHDL
- Basic understanding of C programming

REGISTRATION DETAILS

Registration for the course can be made by sending the duly filled Registration form along with a DD for **Rs.750/- in favor of "The Principal, Kamaraj College of Engineering & Technology, Virudhunagar", payable at Virudhunagar**. Registration Fee includes working lunch, tea and required materials.

HOW TO APPLY

1) **Demand Draft** for **Rs.750/-** should be drawn in favour of **"The Principal, Kamaraj College of Engineering & Technology, Virudhunagar", payable at Virudhunagar**.
2) Send the scanned copy of your DD along with a covering letter duly signed by the Principal of your institution to augustinjacobece@kamarajengg.edu.in on or before July 27, 2015.
3) Sent Original DD to the Coordinator of the Workshop (address mentioned in the front page of the brochure) on or before July 30, 2015.

SCHEDULED DATES

Last date for Registration : 27th July, 2015
Intimation of selection : 29th July, 2015

APPLICATION FORM

Workshop on
System Design Using Vivado Design Suite and Zynq-7000 SoC

Organized by Department of ECE,
kamaraj College of Engineering and Technology
In Association with CoreEL Technologies.
(31st July & 1st August, 2015)

1. Name :
2. Designation :
3. Educational Qualification :
4. Name of the Institute :

5. Address for Communication :

   Email :
   Mobile :
6. Professional Experience :
   Teaching :
   Industry :
7. Accommodation needed: Yes/No

Declaration:
The information furnished above is true to the best of my knowledge.
Date:
Place: Signature of the Applicant

Mr./Ms./Dr._____ is an employee/student of our institute. He / She will be permitted to attend the programme if selected.

Date:
Place:

Signature & Seal
of Head of Organization