A WORKSHOP
on
"Image and Signal Processing Applications using Xilinx System Generator"

(19th – 20th June 2014)

REGISTRATION FORM

Name : _____

Designation: _____

Institution: _____

Address for communication:

_____

_____

_____

Phone Number : _____

E-Mail ID: _____

DD. No: _____

Date: _____

Amount: _____

Bank: _____

Signature

Target participants

Faculty members, Research scholars, M.Tech. Students and Participants from industry.

Registration Fee

Faculty/Industry participants : Rs. 1200/ -
Research scholars/Students : Rs. 800/ -

Registration fee includes registration kit, lunch and refreshment for both the days. Accommodation can be provided upon request on payment basis.

Registration

The Registration form in the prescribed format, along with non-refundable DD drawn in favour of **"IIIT BHUBANESWAR", payable at BHUBANESWAR ,** to be sent to the below mentioned contact address on or before **17th** June **2014**. Seats are limited only.

Organizing Committee

Advisors:

Prof . Gopal Krishna Nayak
Prof . Ajit Kumar Das

Conveners:

Prof. Pradyut Kumar Biswal
Prof. Harish Kumar Sahoo

Members:

Prof. Bijayananda Patanaik
Prof. Subrata Kumar Mohanty
Prof. Rajat Kumar Giri
Prof. C. S. Rao
Prof. Asutosh Kar

Address for Correspondence

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A WORKSHOP
on
Image and Signal Processing Applications using Xilinx System Generator

(19th – 20th June 2014)

Organized by
Department of Electronics & Telecommunication Engineering
IIIT Bhubaneswar
(A University established by Govt. of Odisha)

in association with

CoreEL Technologies
Enabling Excellence

XILINX®

About IIIT Bhubaneswar

International Institute of Information Technology, Bhubaneswar owes its origins to the initiative of the Government of Odisha. It is a result of the desire of the Government to establish a world class institute of Information Technology in the state. The Institute has been converted into a unitary university by the Government of Odisha on 20th Jan 2014.

The Management of the institute is in the hands of a Governing Body, consisting of representatives from the Government of Odisha, Leaders from the IT industry and eminent educationists. Currently, the Chairman of the Institute is the Chief Secretary of the Government of Odisha. IIIT-Bhubaneswar has its focus on quality and rigorous education, quality resource, academic infrastructure, technology and innovation. These initiatives have helped IIIT-Bhubaneswar achieve pre-eminence in India and beyond.

Our vision is to be an unique institute imparting education, training, research, and consulting in technology and related fields to develop human resources who will lead the economy and the society in the coming decades.

About the Department

The Department of Electronics & Telecommunication Engineering has a team ofwell qualified,experiencedand dedicated faculty members with research and teaching backgrounds. The laboratories are well equipped with modern training facilities that cater to the requirements of the students as well as for research activities. This year, the department has planned to start Ph.D. program

About CoreEL Technologies

CoreEL Technologies is a technology company with businesses spread across Design Services & Product Development, Distribution and Training. Head Quartered in Bangalore, India, CoreEL is a leading provider of VLSI & Embedded System design services and Intellectual Property. Since its inception in 1999, CoreEL Technologies a privately held corporation has always strived to deliver quality solutions & support in all the business areas that it serves.

Its Services offerings include Distribution of Silicon solution, EDA tolls, COTS products, Engineering Services (Turn Key Systems Design, Turn Key FPGA Design and High Speed PCB Design), Education and Manufacturing.

About CoreEL University Program

The mission of the University Program from CoreEL is to provide Eco-System support to Indian Academia in Engineering Higher Education in the field of VLSI and Embedded Systems, thereby enabling the delivery of quality education.We achieve this by providing state of the art products from Xilinx, Mentor Graphics and Wind River to Universities. Multi-year application engineering support on these products. Faculty and Students Training Providing Industry Specific Inputs to update the curriculum Helping Universities set-up Centers of Excellence in theVLSI and Embedded Systems arena.

About this Workshop

This workshop allows the participants to explore the Xilinx DSP Design flow with System Generator tool and its integration with MATLAB/Simulink for addressing hardware implementation of DSP & Multimedia (image and signal processing) algorithms using Xilinx FPGA's. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP design implementation and hardware co-simulation verification. Through hands-on exercises, participants can implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities. The program also provides a comprehensive overview of addressing image and signal processing applications using Xilinx Spartan-6 & Virtex-5/6/7 family of FPGA Development platforms.

Course Highlights

- The training program delivers the following key concepts to the participants:
- Introduction to System Generator for DSP
- Concepts of system modeling using Simulink
- Implementing System Control models with the help of Xilinx block sets.
- Implementing Filter Design & perform hardware co-simulation using System Generator
- Introduction of the application based on Signal, Image and Video processing

What you will learn?

After the completion of this training program the participants will be able to:

- Understand why FPGAs are preferred over DSP's to address high performance DSP design implementations
- Describe the basics of system modeling using Simulink
- Narrate the features of Xilinx System generator for DSP
- Model and simulate a system model using Simulink/ System Generator
- Identify the solutions from Xilinx DSP design flow for addressing image, audio and signal processing applications

Pre-requisites

- Concepts of digital design
- Familiarity with HDL (VHDL or Verilog)
- Basic awareness on Xilinx FPGA design flow
- Fundamental Digital Signal Processing

RESOURCE PERSONS

1. Mrs. Sadiya Arsad, National Manager
2. Mr. Samik Basu, Zonal Manager
3. Mr. Prakash G, Product Support Specialist, CoreEL Technologies (I) Pvt. Ltd.