**DSP Design Flow Workshop**

**Atlys Board**

**COURSE DESCRIPTION**

The DSP Design Flow workshop provides an introduction to the advanced tools you need to design and implement DSP algorithms targeting FPGAs. This intermediate workshop in implementing DSP functions focuses on learning how to use System Generator for DSP, as well as HDL design flow, CORE Generator software, and design implementation tools. Through hands-on exercises, you will implement a design from algorithm concept to verification.

# Install Software

The workshop has been tested on a PC running the Windows XP Professional operating system.

* 1. Mathworks tools
     1. release r2010a (includes Matlab/simulink)
     2. Simulink signal processing blockset
  2. Xilinx tools (Professors may submit online donation form at www.xilinx.com/university)
     1. v13.2i ISE Foundation Software
     2. v13.2 System Generator for DSP
  3. Download and install Adept driver and software available at <http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,66,828&Prod=ADEPT2>

1. **Install workshop materials**

The labsource.zip file contains atlys\_board\_plugin.zip, 13\_2\_ISE\_DS\_ISE\_nt\_plugins\_Digilent.zip, and labs.zip files. Unzip this file in temp.

The plugin files are required to enable JTAG and point-to-point Ethernet co-simulation targeting the Atlys board.

* 1. Unzip atlys\_board\_plugin.zip file in <xilinx13\_2>\ISE\_DS\ISE\sysgen\plugins\compilation\Hardware Co-Simulation directory
  2. Unzip 13\_2\_ISE\_DS\_ISE\_nt\_plugins\_Digilent.zip file in <xilinx13\_2>\ISE\_DS\ISE\lib\nt\plugins directory
  3. Verify installation
     1. Start Matlab 2010a and enter **simulink** at the matlab command prompt to invoke simulink
     2. Expand the Xilinx blockset and select Basic Elements
     3. Double-click on the System Generator token
     4. Select Hardware Co-Simulation as the compilation type and select Atlys board. The following options should be selected and grayed out
        + Part: Spartan6 xc6slx45-2csg324 device
        + FPGA clock period (ns): 10
        + Clock pin location: fixed

The labs.zip file consists of source files needed to conduct labs. Unzip the labs.zip file in c:\xup\dsp\_flow\ directory.

The docs\_pdf.zip file contains lab documents and presentations in PDF format. Unzip this file in c:\xup\dsp\_flow or any other directory of your choice.

1. **Setup the hardware**

Connect and power the Atlys board

* 1. Connect up the Atlys board
     1. Connect the power supply
     2. Connect the USB download cable between the JTAG configuration port of the board and USB connection on the PC
  2. Power up the board

1. **For Professors only**

Download the labsolution.zip and docs\_source.zip files using your membership account. Do not distribute them to students or post them on a web site. The docs\_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get started**

Review the presentation slides and complete the lab exercises according to the workshop flow shown below.

1. **Contact XUP**

Please email [xup@xilinx.com](mailto:xup@xilinx.com) with questions or comments

# Workshop Flow

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| **Day 1 Agenda** | **Day 1 Materials** |
| FPGAs for DSP | 01\_intro.pptx |
| Introduction to System Generator for DSP | 02\_Intro\_SysGen.pptx |
| Simulink Basics | 03\_Simulink\_Basic.pptx |
| Lab 1 introduction | 03a\_Lab1\_Intro.pptx |
| Lab 1: Brief introduction to Simulink | lab01.docx (lab 1 instructions)  /labs/lab1 (lab 1 “user” directory)  /labsolution/lab1 (lab 1 solutions) |
| Basic Xilinx Design Capture | 04\_Basic\_XDC.ppt |
| Lab 2 introduction | 04a\_Lab4\_Intro.ppt |
| Lab 2: Getting Started w/ System Generator | lab02.docx (lab 2 instructions)  /labs/lab2 (lab 2 “user” directory)  /labsolution/lab1 (lab 2 solutions) |
| Signal Routing | 05\_Signal\_Routing.pptx |
| Lab 3 introduction | 05a\_Lab3\_Intro.pptx |
| Lab 3: : Signal Routing | lab03.docx (lab 3 instructions) |
| **Day 2 Agenda** | **Day 2 Materials** |
| Implementing System Control | 06\_System\_Control.pptx |
| Lab 4 introduction | 06a\_Lab4\_Intro.pptx |
| Lab 4: Implementing System Control | lab04.docx (lab 4 instructions) |
| Multi-Rate Systems | 07\_Multirate\_Systems.pptx |
| Lab 5 introduction | 07a\_Lab5\_Intro.pptx |
| Lab 5: Designing a MAC FIR | lab05.docx (lab 5 instructions) |
| Multi-rate systems | 08\_Filter\_design.pptx |
| Lab 6 introduction | 08a\_Lab6\_Intro.pptx |
| Lab 6: Designing a FIR Filter | lab06.docx (lab 6 instructions) |