**Partial Reconfiguration Flow Workshop**

**Genesys Board**

**COURSE DESCRIPTION**

Partial Reconfiguration Flow workshop provides professors with an introduction to the partial reconfiguration design flow in Xilinx FPGAs. It covers basic terminologies used in partial reconfiguration, provides understanding of the fundamental steps involved in developing a design capable of partial reconfiguration. You will learn the capabilities of and restrictions imposed by the reconfiguration tools. You will use Xilinx EDK, Software Development Kit (SDK), and PlanAhead tools to design and develop partial reconfiguration capable designs.

# Install Xilinx software

Professors may submit the online donation request form at [www.xilinx.com/univ](http://www.xilinx.com/univ) to obtain the latest Xilinx software. The workshop was tested on a PC running MicroSoft Windows XP professional edition. Debug is verified using hyperterminal.

* V12.3 ISE Foundation Software
* V12.3 Chipscope-Pro
* V12.3 EDK
* V12.3 PlanAhead
1. **Setup hardware**

Connect Genesys Board

* 1. Connect programming cable between configuration port of Genesys Board and PC
	2. Connect RS232 serial cable between Genesys Board and PC serial ports
	3. Connect the power supply and power on the board
1. **Install distribution**

Extract the labsource.zip file in c:\xup\PartialReconfiguration directory.

The docs\_pdf.zip file consists of lab documents and presentations in PDF format. Extract this zip file in c:\xup\ PartialReconfiguration \ directory or any directory of your choice.

1. **For Professors only**

Download the docs\_source.zip file using your membership account. Do not distribute them to students or post them on a web site. The docs\_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom. Note: labsolution.zip is not available due to its size of about 1.8 GB

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

1. **Contact XUP**

Send an email to xup\_pr@xilinx.com for questions or comments