**Advanced Embedded System Design on Zynq Using Vivado Workshop**

**ZedBoard**

**COURSE DESCRIPTION**

This workshop provides participants the necessary skills to develop complex embedded systems and enable them to improve their designs by using the tools available in Vivado. It also helps developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq™ All Programmable System on a Chip (SoC).

# Install Xilinx software

Professors may submit the online donation request form at <http://www.xilinx.com/member/xup/donation/request.htm> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2016.1 System Edition
* Download and install software driver, for serial communication using micro-USB cable, available at <http://www.zedboard.org>
1. **Setup hardware**

Connect ZedBoard

* 1. Connect programming cable between configuration port of ZedBoard and PC
	2. Connect another micro USB cable between ZedBoard’s UART port and PC USB port
	3. Connect the power supply and power on the board
1. **Install distribution**

Extract the **2016\_1\_zynq\_sources.zip** file in the *c:\xup\adv\_embedded* directory. This will create a **sources** folder. Create the *c:\xup\adv\_embedded\2016\_1\_zynq\_labs* directory. This is where you will do the labs. The **2016\_1\_zynq\_labdocs\_pdf.zip** file consists of lab documents in the PDF format. Extract this zip file in *c:\xup\adv\_embedded* directory or any other directory of your choice.

1. **For Professors only**

Download the **2016\_1\_zed\_labsolution.zip** and **2016\_1\_zynq\_docs\_source.zip** files using your membership account. Do not distribute them to students or post them on a web site. The **2016\_1\_zynq\_docs\_source.zip** file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| Embedded System Design Review  | 11\_embedded\_system\_design\_review.ppt x |
| Lab 1: Building a Complete Embedded System  | 11a\_lab1\_intro.pptxLab1.docx |
| Advanced Zynq Architecture  | 12\_Advanced\_Zynq\_Architecture.pptx |
| System Debugging  | 13\_System\_Debugging.pptx |
| Lab 2: Debugging using Vivado Logic Analyzer | 13a\_lab2\_intro.pptxLab2.docx |
| Memory Interfacing  | 14\_Memory\_Interfacing.pptx |
| Lab 3: Extending Memory Space with Block RAM | 14a\_lab3\_intro.pptxLab3.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Interrupts | 15\_ Interrupts.pptx |
| Low Latency High Bandwidth | 16\_Low\_Latency\_High\_Bandwidth |
| Lab 4: Direct Memory Access using CDMA  | 16a\_lab4\_intro.pptxLab4.docx |
| Configuration and Bootloading | 17\_Configuration\_and\_Bootloading.pptx |
| Lab 5: 17\_Configuration\_and\_Bootloading | 17a\_lab5\_into.pptxLab5.docx |
| Profiling and Performance Improvement | 18\_Profiling\_and\_Performance\_Improvement.pptx |
| Lab 6: Profiling and Performance Tuning | 18a\_lab6\_intro.pptxLab6.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Create a complete processor system with built-in processor and IP in programmable logic.

Lab 2 - Insert various debug cores to debug/analyze system behavior.

Lab 3 - Instantiate AXI BRAM controller and BRAM to extend address space and run application from it.

Lab 4 - Perform DMA operations between various memories using AXI CDMA controller in polling and interrupt modes.

Lab 5 - Create images to boot off the SD card and QSPI flash. Load previously generated hardware bitstreams and executable and execute desired application.

Lab 6 - Profile an application performing a function both in software and hardware.

1. **Contact XUP**

Send an email to xup@xilinx.com for questions or comments