**FPGA Design Flow using Vivado Workshop**

**NEXYS VIDEO**

**COURSE DESCRIPTION**

The purpose of this workshop is to introduce digital designers to the FPGA design flow using Vivado design tool. During the course of the workshop, the user will step through the complete Xilinx design flow from design entry to download. The workshop includes slides and labs to help guide the user through the flow.

# Install Xilinx software

Professors may submit the online donation request form at <http://www.xilinx.com/member/xup/donation/request.htm> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2016.2 System Edition

1. **Setup hardware**

Connect NEXYS VIDEO

* 1. Set the power supply jumper to USB so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable
  2. Connect micro USB cable between PROG UART port of NEXYS VIDEO and PC

1. **Install distribution**

Extract the **2016\_2\_artix7\_sources.zip** file in the *c:\xup\fpga\_flow* directory. This will create a **2016\_2\_artix7\_sources** folder. Create the **c:\xup\fpga\_flow\2016\_2\_artix7\_labs** directory. This is where you will do the labs. The **2016\_2\_artix7\_labdocs\_pdf.zip** file consists of lab documents in the PDF format. Extract this zip file in the *c:\xup\fpga\_flow* directory or any other directory of your choice.

1. **For Professors only**

Download the **2016\_2\_nexysvideo\_labsolution.zip** and **2016\_2\_artix7\_docs\_source.zip** files using your membership account. Do not distribute them to students or post them on a web site. The **2016\_2\_artix7\_docs\_source.zip** file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| 7-Series Architecture Overview | 11\_7\_Series\_Architecture\_Overview.ppt x |
| Vivado Design Flow | 12\_ Vivado Design Flow.pptx |
| Lab 1: Vivado Design Flow | 12a\_lab1\_intro.pptx  Lab1.docx |
| Synthesis | 13\_Synthesis.pptx |
| Lab 2: Synthesizing a RTL Design | 13a\_lab2\_intro.pptx  Lab2.docx |
| Implementation and STA | 14\_ Implementation\_and\_STA.pptx |
| Lab 3: Implementing and Verify the design in hardware | 14a\_lab3\_intro.pptx  Lab3.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| IP Integrator and IP Catalog | 15\_ IPI\_and\_IP\_Catalog.pptx |
| Lab 4: Using IP Catalog | 15a\_lab4\_intro.pptx  Lab4.docx |
| Xilinx Design Constraints | 16\_Xilinx\_Design\_Constraints.pptx |
| Lab 5: Xilinx Design Constraints | 16a\_lab5\_into.pptx  Lab5.docx |
| Hardware Debugging | 17\_Hardware\_Debugging.pptx |
| Lab 6: Hardware Debugging | 17a\_lab6\_intro.pptx  Lab6.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Vivado Design Flow: Use Vivado IDE to create a simple HDL design targeting the NEXYS4.

Lab 2 - Synthesizing a RTL Design: Synthesize a design with the default settings as well as some settings changed and observe the effect.

Lab 3 - Implementing and verify the design in hardware: Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.

Lab 4 - Using IP Catalog: Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.

Lab 5 - Xilinx Design Constraints: Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the timing analysis.

Lab 6 - Hardware Debugging: Use Mark Debug feature and also available Integrated Logic Analyzer (ILA) core (available in IP Catalog) to debug the hardware.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments