**High-Level Synthesis Flow on Zynq using Vivado HLS Workshop**

**ZedBoard**

**COURSE DESCRIPTION**

This course provides professors with an understanding of high-level synthesis design methodologies necessary to develop digital systems using Vivado HLS. After completing this workshop, you will be able to understand high-level synthesis flow of Vivado HLS, apply appropriate directives to optimize design performance, and create a custom peripheral and add it to a processor system.

# Install Xilinx software

Professors may submit the online donation request form at <https://www.xilinx.com/support/university/donation-program.html> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2017.4 System Edition

1. **Setup hardware**

Connect ZedBoard

* 1. Connect programming cable between configuration port of ZedBoard and PC
  2. Connect the power supply and power on the board

1. **Install distribution**

Extract the **labsource.zip** file in the *c:\xup\hls* directory. This will create a **labs** folder. The **labdocs.zip** file consists of lab documents in the PDF format. Extract this zip file in *c:\xup\hls* directory or any other directory of your choice.

1. **For Professors only**

Download the **labsolution.zip** and **docs\_source.zip** files using your membership account. Do not distribute them to students or post them on a web site. The **docs\_source.zip** file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom. Note: labsolution.zip is not available due to its size.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

|  |  |
| --- | --- |
| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| Introduction to High-Level Synthesis | 11\_HLS\_Intro.ppt x |
| Using Vivado HLS | 12\_Using\_VivadoHLS.pptx |
| Lab 1: Vivado HLS Design Flow | 12a\_lab1\_intro.pptx  01\_Lab.docx |
| Improving Performance | 13\_Improving\_Performance.pptx |
| Lab 2: Improving Performance | 13a\_lab2\_intro.pptx  02\_Lab.docx |
| Data Types | 14\_Data\_Types.pptx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Optimizing for Area and Resources Utilization | 21\_Improving\_Resources.pptx |
| Lab 3: Improving Area and Resources Utilization | 21a\_lab3\_intro.pptx  03\_Lab.docx |
| IO Protocols | 22\_IO\_Protocols.pptx |
| Coding Considerations | 23\_Coding\_Considerations.ppt |
| Creating a Processor System | 24\_Creating\_Processor\_System.pptx |
| Lab 4: Creating a Processor System to Filter Audio Signal | 24a\_lab4\_into.pptx  04\_Lab.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Experience a basic design flow of Vivado HLS and review generated output.

Lab 2 - Use pipelining technique to improve performance.

Lab 3 - Use directives to optimize resource sharing.

Lab 4 - Use IP-XACT export capability of Vivado HLS to generate an IP and integrate the generated core in an embedded system developed using IP Integrator.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments