**System Design Flow on Zynq using Vivado Workshop**

**ZedBoard**

**COURSE DESCRIPTION**

This course provides professors necessary skills to design and debug a system using Vivado IP Integrator, hardware analyzer, and Vivado HLS.

# Install Xilinx software

Professors may submit the online donation request form at <http://www.xilinx.com/member/xup/donation/request.htm> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* Vivado 2013.4 System Edition
* Download and install software driver, for serial communication using micro-USB cable, available at <http://www.zedboard.org>
1. **Setup hardware**

Connect ZedBoard

* 1. Connect programming cable between configuration port of ZedBoard and PC
	2. Connect another micro USB cable between ZedBoard’s UART port and PC USB port
	3. Connect the power supply and power on the board
1. **Install distribution**

Extract the labsource.zip file in c:\xup\sys\_design directory. This will generate **sources** and **labs** folders. The labdocs.zip file consists of lab documents in the PDF format. Extract this zip file in c:\xup\sys\_design\ directory or any directory of your choice.

1. **For Professors only**

Download the labsolution.zip and docs\_source.zip files using your membership account. Do not distribute them to students or post them on a web site. The docs\_source.zip file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| 7 Series Architecture Overview  | 11\_7\_Series\_Architecture\_Overview.ppt x |
| Vivado Design Flow | 12\_Vivado Design\_Flow.pptx |
| Lab 1: Synthesizing a RTL Design  | 11a\_lab1\_intro.pptxLab01.docx |
| Xilinx Design Constraints | 13\_Xilinx\_Design\_Constraints.pptx |
| Lab 2: Xilinx Design Constraints | 13a\_lab2\_intro.pptxLab02.docx |
| IP Integrator and Embedded System Design Flow | 14\_IPI\_And\_Embedded\_System\_Design.pptx |
| Lab 3: Create a Processor System using IP Integrator | 14a\_lab3\_intro.pptxLab03.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Creating and Adding Custom IP | 21\_Creating\_and\_Adding\_Custom\_IP.pptx |
| Lab 4: Creating and Adding Custom IP in PL | 21a\_lab4\_intro.pptxLab04.docx |
| System Debugging | 22\_System\_Debugging.pptx |
| Lab 5: System Debugging using Vivado Logic Analyzer and SDK | 22a\_lab5\_into.pptxLab05.docx |
| Profiling and Performance Improvement | 23\_Profiling\_and\_Performance\_Improvement.pptx |
| Introduction to High-Level Synthesis with Vivado HLS | 24\_Vivado\_HLS\_Intro.pptx |
| Improving Performance and Resource Utilization | 25\_Improving\_Performance\_and\_Resource\_Utilization |
| Creating an Accelerator | 26\_Creating\_an\_accelerator.pptx |
| Lab 6: Creating a Processor System | 26a\_lab6\_into.pptxLab06.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Use Vivado IDE to create a simple HDL design. Simulate the design using the XSim HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.

Lab 2 - Create a project with I/O Planning type, enter pin locations, and export it to the RTL. Then create the timing constraints and perform the timing analysis.

Lab 3 – Create a simple ARM Cortex-A9 based processor design targeting the ZedBoard using IP Integrator.

Lab 4 - Use the Manage IP feature of Vivado to create a custom IP and extend the system with the custom peripheral. Write a basic C application to access the peripherals.

Lab 5 - Insert various Vivado Logic Analyzer cores to debug/analyze system behavior.

Lab 6 - Profile an application performing a function both in software and hardware. Create an accelerator in Vivado HLS. Use the generated accelerator to build a complete system.

1. **Contact XUP**

Send an email to xup@xilinx.com for questions or comments