## Revision History

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<td><strong>08/16/2019 Version 1.2</strong></td>
<td></td>
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<tr>
<td>Working with the RF Analyzer</td>
<td>Added sub-topics to include detail about installation, generation, and acquisition.</td>
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<tr>
<td><strong>12/14/2018 Version 1.1</strong></td>
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<tr>
<td>Chapter 1: Introduction</td>
<td>Added information about supported features.</td>
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<td>File Menu Options</td>
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<td>Settings Menu Options</td>
<td>Updated information about the Communication and Analysis settings menu options.</td>
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<td>RF-DAC Output Settings</td>
<td>Updated the section and DAC Current Mode screen capture.</td>
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<td>Power Advantage Tool</td>
<td>Added new section.</td>
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<tr>
<td>Chapter 4: Tabs</td>
<td>Updated the MemType section and added information about the size limitation in the DDR mode.</td>
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<td>FFT Page</td>
<td>Added information about Zoom Tools.</td>
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<td><strong>10/19/2018 Version 1.0</strong></td>
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<tr>
<td>Initial release.</td>
<td>N/A</td>
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Chapter 1

Introduction

This document describes the RF Data Converter user interface used to drive and analyze the Zynq® UltraScale+™ RFSoC. This general user interface communicates seamlessly with the help of an open communication protocol used on the ZCU111 RF Data Converter (RFDC) Evaluation Tool and on the RF Analyzer for signal generation through RF-sampling digital-to-analog converters (RF-DACs), data capturing through RF-sampling analog-to-digital converters (RF-ADCs), and following fast Fourier transform (FFT) analysis as well as its main RF data converter metrics. This document focuses on the usage of this software GUI only.


For the RF Analyzer, this GUI is the main debug interface. For use with the RF Analyzer, all board control functions, including clock configuration, RF-DAC current mode control, and external interface configuration, are not available. The clock scheme used with the RF Analyzer belongs to the Vivado tools IP configuration.

The highlights of the RF Data Converter user interface are listed here:

1. Ability to control all RF-ADC and RF-DAC channels operating at the same time.
2. Ability to customize and control the data converter sample frequency using either internal or external clocking.
3. Direct API function access.
4. Save and restore of configurations and preferences that enables quick settings.
5. Synchronized data transmission and capturing enabled with multi-tile synchronization (MTS).
6. Import and export of data waveform with LVM (ASCII) and TDMS (binary) file format.
7. Data length of transmission and capturing is up to 64M samples (DDR mode).
The following table compares the features that this software GUI supports with the Evaluation Tool and RF Analyzer.

**Table 1: Feature Support**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Evaluation Tool</th>
<th>RF Analyzer</th>
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<tbody>
<tr>
<td>Communication Interface</td>
<td>Ethernet</td>
<td>JTAG-UART</td>
</tr>
<tr>
<td>Board Support</td>
<td>ZCU111</td>
<td>Any Zynq UltraScale+ RFSoC based board</td>
</tr>
<tr>
<td>Memory</td>
<td>DDR and BRAM</td>
<td>BRAM only</td>
</tr>
<tr>
<td>External Component Support</td>
<td>External PLL, RF-DAC Power supply</td>
<td>None</td>
</tr>
<tr>
<td>Multi-Tile Synchronization (MTS) Support</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Multi-Band Support</td>
<td>Yes</td>
<td>Yes with pre-built bitstreams</td>
</tr>
</tbody>
</table>
Chapter 2

Software Installation

1. The Vivado® Design Suite (2018.2 or later version) must be installed on the host.
2. Run the installer supplied with the tool (RFDC Evaluation or RF Analyzer). This installer requests the LabVIEW run-time engine. If the run-time engine is not already installed and is not present in the downloaded package, use the link supplied here to download the correct version: LabVIEW Run-Time Engine 2017 SP1.
Menu

File Menu Options

- **File → Load/Save configuration**: Configuration covers all the displayed settings of the Zynq® UltraScale+™ RFSoC such as, real or I/Q mode, mixer settings, and enable or bypass internal PLL. All these settings can be saved and restored. This feature enables quick configuration as well as configurations that can be shared with others. Configuration files are located in \Config\ directory, with the file extension of .cfg.

- **File → Load/Save preferences**: Preferences are the user-defined settings of the GUI. It includes tabs used for data generation, data capture, and user options in the GUI that are not linked to the device under test (DUT) configuration such as, mapping in the MultiView mode, number of samples, and tone frequency. You can save the preferred settings of GUI or restore any of them. Preferences files are located in \Config\ directory, with the file extension of .prf.

- **File → Hardware target**: RF Analyzer only. Opens the bitstream download screen.

- **File → Export ADC Data**: This command exports the RF-ADC data captured of all the opened RF-ADC channels with LVM or TDMS file format (chosen in Settings → Data File Format). The default directory is \Data\ADC\.

- **File → Exit**: Exit the software.

Edit Menu Options

- **Edit**: Standard Windows edit menu.
Settings Menu Options

- **Settings → Communication**: Displays the current communication interface. Ethernet for the Evaluation Tool and JTAG-UART for the RF Analyzer.

  *Figure 1: Communication Interface*

- **Settings → Analysis**: Some RF-ADC metrics are based on the frequency range. On the RF-ADC FFT page, there is a marked out calculation table, the SNR, ENOB, SFDRxH23, and FspurxH23 are calculated based on the Band of Interest set here. In loop mode, some metrics are calculated over a number of measurements that can be set under Averaging.
• **Settings → Data Folders**: Select your preferred folders for the test vector of RF-DAC, saved data from RF-ADC, and onboard clocking frequency configuration files. By default, these are located in `\Data\`, with ADC, DAC, and Clocking as the respective folder names.

• **Settings → Data File Format**: Indicate your preferred file format between the `.lvm` and `.tdms` formats. For the RF-ADC data output, you can select Data and Metrics when you click export ADC data in the File menu.
Window Menu Options

- **Window → MultiView**: The MultiView option opens all the RF-ADC or RF-DAC FFT diagrams on a single page with customized channels. Click *Generate/Acquire All* to update all the windows.

*Figure 4: MultiView RF-ADC FFT*

To display all the RF-ADC channel signals in the time domain, select the **ADC Time Domain** option. This feature is particularly useful in the MTS mode.

*Figure 5: MultiView RF-ADC Time Domain*
• **Window → Commands log:** This opens the commands log window where the history for all the commands can be seen, the API can be run, and feedback can be viewed. If an error occurs with the GUI, it appears on the command log. The command log window can also be used to create a dump file which lists out all the previously used commands. This can be useful in debugging if an error occurs with a sent command.

![Command Window](image)

**Figure 6: Command Window**

• **Window → Merge all windows:** Opened tabs can be moved to separate windows. This command merges all the separate windows into one.

---

**Help Menu Options**

• **Help → About:** Provides general information about the RF Data Converter evaluation tool. Use this option to check the version, which is required when building the `.lvm` file.
**Chapter 4**

# Tabs

Overview is the home page of the RF Data Converter evaluation tool GUI. It displays the top framework of all the converters grouped by tile. This page is displayed upon startup and cannot be closed.

**MemType**

In the overview tab (only available with the RF evaluation tool), select MemType to choose the memory type, **BRAM** (on Zynq® UltraScale+™ RFSOC) or **DDR** (on the ZCU111 evaluation board). DDR is bigger in size than BRAM.

The maximum sample size allowed is dependent on the design. The design return an error or a warning if the maximum size is exceeded. The DDR mode supports up to 128M samples per channel, but has limitations on the data rates. This limitation on the data rates comes from different aspects of the software design and not from the Zynq UltraScale+ RFSOC.
Onboard Clocking

The onboard clocking tab is only available with the RF evaluation tool. In the overview tab, select Clock Settings to open the onboard PLL GUI in the right panel. This GUI allows you to control and set the input as well as output frequencies for the PLLs that are integrated onto the ZCU111 evaluation board. This GUI provides the Predefined and Advanced mode options for onboard clock setting. Both the configuration options allow full rate sampling clock outputs of up to 4 GHz for the RF-ADC and 6.554 GHz for the RF-DAC directly, or low frequencies such as 245.76 MHz as the input reference of the on-chip PLLs. In the Predefined mode, available frequencies are provided in the drop-down list for RF-ADC and RF-DAC. Choose the options you would like and click Apply. The GUI programs the onboard RFPLLs. If your desired frequency does not appear in the predefined list, then you must use the advanced configuration mode to customize the sample rates.

Figure 7: Onboard PLL Predefined

The Advanced mode accepts the configuration file for all four clock chips (LMK04208 and LMX2594) for individual control. You can choose the .tcs file shipped along with this tool or generate your own configuration files using TICS Pro Software. See Appendix A: Customization and Testing for an example of this procedure.

Twenty-two pre-generated configuration files of LMX2594 are shipped with this software located in the `\Data\Clocking\` folder. These pre-generated configuration files are based on the reference clock of 122.88 MHz.

Click Advanced to select the desired clock configuration.
Related Information
Customize Clock Frequencies

RF-DAC Output Settings

RF-DAC output current settings are only available with the RF evaluation tool. In the overview tab, click the **Power Settings** button to open the RF-DAC output settings page in the right panel. Choose from the available 20 mA/2.5V and 32 mA/3.0V options. Power supply for this current mode control (DAC_AVTT) is programmable on the board through the power management unit (PMU). Click **Apply** to program the onboard PMU for either 2.5V or 3.0V, and switch to the corresponding RF-DAC output current mode.
Power Advantage Tool

The power advantage tool is integrated in this software to provide power related information for reference. This power advantage tool displays voltage, current, and power information for each rail that is monitored by the onboard power management unit. The power advantage tool communicates with the evaluation software through the JTAG interface. To retrieve the power information, connect the JTAG port to the host.

Figure 10: Power Advantage Tool
RF-ADC/RF-DAC Tile

In the overview tab, selecting any of the RF-ADC or RF-DAC tile opens the individual tile page as illustrated in the following figure. In this tab, you can reset, shut down, start up a tile, and also view the current tile status by clicking Refresh. When a tile is in operation, selecting Tile settings opens up the configuration tab for it. Refer to the Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269) for more information on the commands and power up state machine status.
Tile PLL Settings

In the tile PLL setting page, click on the PLL box to open the PLL settings in the right panel. The onboard PLL (LMX2594), or external, can be selected as the clocking source for the converter tile input reference. For the RF Analyzer, only the external option is available.

Figure 12: Tile Status

Figure 13: Internal PLL
If the external clocking source is selected, a capacitor is required to be soldered on the board (refer to the ZCU111 Evaluation Board User Guide (UG1271) for details). Feed the clock through the XM50x daughter card, and disable the related output from the onboard RFPLL. Ensure that the correct clock frequency being supplied from the external source is input.

**Note:** 0 dBm is required to drive Zynq® UltraScale+™ RFSoC clock input for optimized performance. Insertion loss must be taken into account when clocking the Zynq UltraScale+ RFSoC directly through the XM50x evaluation board. Insertion loss could be high at full sampling frequency.

Ensure that the input clock rate is correct for the internal PLL, enabled or bypassed. When bypassing the internal PLL, the input clock functions as a sampling clock of the converter, which in general amounts to several GHz. When the internal PLL is enabled, ensure that the input frequency is within the range specified by the Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926). A reference frequency can also be typed in when the internal PLL is disabled. This helps the GUI calculate the reference spurs on the FFT page.

For enabling the internal PLL, input the desired sampling frequency, and then click **Apply**. The driver through the Xrfdc_DynamicPLLConfig function, automatically calculates and displays the values of the input reference divider, feedback divider, and output divider. The lamp lights up green after the PLL is successfully locked.

---

**Converter Settings**

In each RF-ADC/RF-DAC tile, the available converter channels and associated internal function blocks are cascaded in the block diagram, and the text shows the current settings. Click any function block to open the config page in the right panel. FIFO and Crossbar have their own separate pages.
**RF-ADC Settings**

- **Calibration Mode**: Selects between different calibration optimization schemes depending on the features of the input signals. Mode 1 is optimal for input frequencies $F_{\text{samp}}/2$ (Nyquist) +/- 10%. Otherwise, use Mode 2.

**Figure 15: Calibration Mode**

- **Nyquist Zone**: Choose the Nyquist zone in which the input signal located. This is related to interleaving calibration and must be indicated correctly. Zone 1 is for odd and Zone 2 is for even.

- **Threshold Detection**: Use this to set the embedded threshold detection parameter.
• **Decimation Settings:** Use this to select the decimation factor. Do not select Off or you will not receive any data. It is recommended that the same decimation factor is used for all data converters in the tile to avoid potential timing issues.

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**RF-DAC Settings**

• **Decoder Mode:** Choose which performance to optimize, noise floor or linearity. Noise floor optimization must be selected for communication applications.

• **Nyquist Zone:** Choose which Nyquist zone the signal will be located in, Normal Mode for Nyquist zone one and Mix Mode for Nyquist zone two. See this link for more information.

• **Interpolation Settings:** Choose your interpolation factor. Do not select off or some digital blocks will be powered down and you will not receive the outputs.

• **Inverse Sinc Settings:** Enabling Inverse Sinc compensates sinc roll-off at high frequencies. This function is only effective when the signal is located in Nyquist zone one.

---

**Settings in RF-ADC and RF-DAC**

• **Mixer Settings:** Set the Crossbar page first, then set other parameters of the mixer and NCO because mixer is bypassed in the real-to-real mode.

• **QMC Settings:** QMC module contains gain, phase, and DC-offset adjusting. These are used to compensate unmatched I and Q signal path when converters interface to external modulators or demodulators. DC offset takes effect with DC coupling only. Phase offset takes effect with complex mode only. Gain take effects in all modes.

• **FIFO:** Show the FIFO clock rates and number of words on PL and converter side for information only.
Crossbar

Click the Crossbar button at the bottom of the converter settings page, or, alternatively, the Crossbar box in the left panel to display the crossbar page. This page determines the real or complex mode of the mixer and multi-bands operating mode. Complex mode activates a pair of channels to support both in-phase(I) and quadrature(Q) signal. Because of the complex mixer (and NCO) architecture, the real-to-complex (R2C) or complex-to-complex (C2C) mode is allowed, but complex-to-real (C2R) mode is not allowed. This means that there is no C2R mode available for RF-ADC and no R2C mode available for RF-DAC. Correct operating modes are ensured by this tool. In complex mode, even channels are always used for I signals and odd channels are used for Q signals.

Figure 16: Crossbar
Multi-Bands

Multiple bands enable one RF-DAC or RF-ADC analog channel and share multiple DUC or DDC channels to transmit or receive the multi-band carrier signals. For RF-DAC, multiple baseband signals can be up-converted in separate DUC chains and then combined at the crossbar before being sent to the analog RF-DAC block.

In RF-ADC, the multi-band/carrier inputs from one RF-ADC are split into multiple DDC paths for down-conversion. The carriers from different bands are separated and located at low frequencies (in general at zero). In the multi-bands operation, a converter is enabled on channel 0 (dual bands at channel 0 and 1) or channel 2 (dual bands at channel 2 and 3). Multi-bands operations support both real and complex output. All these configurations can be enabled at the crossbar page. The following figure illustrates the dual bands configuration of C2C and C2R.

Figure 17: Multi-Bands

FFT Page

Click Acquisition in the ADC settings page, or Generation in the DAC settings page, to open the FFT page. In the RF-DAC FFT page, the single tone and dual tone generator is embedded in the software. To generate a complex modulated signal, load the test vector file. There are variations of sub-menus in this page, including signal characteristics, customizing FFT plot, windowing function, test vector input, and output. When decimation or interpolation is enabled in the RF-
ADC or RF-DAC data path, with a value more than 1 (bypass), Eff.Fs and Fs show different values in this table. Fs indicates the sampling frequency of observed RF-ADC or RF-DAC. Eff.Fs indicates the sampling frequency of original data stream (base band) after decimation or before interpolation. The X-axis (frequency) of the FFT plot reflects back the Eff.Fs. The following figure shows the RF-ADC FFT page.

**Figure 18: RF-ADC FFT Page**

Major functions and sub-menus in the FFT page are shown in the following figure.

**Figure 19: FFT Page Sub-Menu**
**Note:** When evaluating RF-ADC performance, note that the Window function can cause some performance value degradation and this is not compensated for in this software. The NSD degrades to around 2 dB when the window function is enabled.

The following figure shows the Zoom Tools on the FFT page. Use the default Zoom Tools or edit the axis range to directly configure the start and/or end values for best plot observation.

*Figure 20: FFT Zoom Tool*

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**Multi-Tile Synchronization**

The multi-tile synchronization (MTS) feature enables multiple converter channels working with an aligned and deterministic latency across tiles and chips. MTS is only supported with the RF evaluation tool. In the overview page, there is an MTS tab on the right corner of the ADC and DAC group. Click the MTS tab to open the function window.
To enable the MTS function, check **enable** → **Apply**. This enables the internal clock scheme to support MTS. After MTS is enabled, select **Synchronise** to implement the alignment and display the measured latency of each tile. An offset value also shows how many T1 (period of sampling clock) offset have been applied to align the tiles. The error lamp lights up red if there are any errors during MTS.

**Figure 21: MTS**

**Figure 22: MTS Successful**
RF Analyzer

Overview

The RF Analyzer provides an easy and fast way to evaluate the performance of RF-ADCs and RF-DACs in the Zynq® UltraScale+™ RFSoC. The bit stream is independent of the evaluation board and external devices, thus the following board related configurations are not available in the GUI.

- Power settings
- External clock settings
- Programmable logic (PL) settings

Working with the RF Analyzer

The RF Analyzer requires that either the 2018.3 HW server or the Vivado® Design Suite (2018.3 or later version) is installed on the host. Ensure that the external clocks are stable before downloading the bitstream based on the actual hardware design. The corresponding converter tiles might show an error if there are no valid clocks available when the converter IP starts up. When using the RF Analyzer with Xilinx® evaluation boards, such as the ZCU1254 or ZCU1275, the System Controller User Interface tool can be used to configure the onboard clocks in advance. See the ZCU111 System Controller – GUI Tutorial (XTP517) for details.

Installing the RF Analyzer

1. Double-click Setup_RF_Analyzer_<version>.exe (you might have to right-click and select Run as Administrator).
2. Select the folder where the RF Analyzer is to be installed.
3. Click **Next** in the following screens, and then select **Install**.

   ![LabVIEW runtime installation screen]

   The LabVIEW runtime installs automatically, if necessary.

4. Restart your computer to complete the installation.

5. To launch the RF Analyzer, double-click the RF_Analyzer application in the installation directory.
Setting the Vivado Path

When the RF Analyzer starts up for the first time, it looks for the Vivado Design Suite. If there is no Vivado Design Suite or HW server directory specified in the `RF_Analyzer.ini`, a window asking for the path of Vivado Design Suite pops open.

1. In the Vivado Directory Selection, browse to the folder where the Vivado Design Suite or HW server is installed.

   ![Vivado Directory Selection](image)

2. Click OK. This directory is recorded in the `RF_Analyzer.ini` for further applications.

Selecting the Hardware Target and Bitstream

The RF Analyzer start screen allows you to configure the hardware target (board).

1. In the Connect to: dialog box, select the connection type as Local or Remote.
2. In the Hardware dialog box, you can see the automatically detected cables and JTAG chain.
3. In the Bitstream Path dialog box select the bitstream. A pre-built bitstream for each supported part is available in the install folder under `\Protocol\RF_Analyzer\bitstreams`. These bitstreams provide the maximum RF configuration flexibility. You can also use your own bitstream by customizing and generating the RF DC IP in the Vivado® Design Suite (see the Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269) for information on generating the RF Data Converter IP core).
After the bitstream download is complete, the RF Analyzer sets up a connection with the Zynq® UltraScale+™ RFSoC, and refreshes the status of the GUI. The following overview page shows up if there are no errors. Device information and the green communication OK bulb appears on the status bar at the bottom of the overview page. The active RF-ADC or RF-DAC tiles might be different based on your actual hardware configuration.
Configuring the Sample Clock

The RF Analyzer cannot acquire the absolute values of tile input clocks and sampling clocks from the IP configuration. Therefore, it is important to configure the sampling clocks before other operations, if these clocks are different to the initial IP configuration.

1. Double-click on an ADC or a DAC tile.

2. Select the PLL and configure the clocks based on the hardware design.
3. Click **Apply**.

**RECOMMENDED:** Configure clocks for each active tile before performing other operations.

### Sample Clocks Configuration

- **Clocking Reference:** This frequency is only used to calculate reference spurs in the RF-ADC FFT page. When sampling frequency is fed directly from an external clock, the clocking reference is the reference clock of the external clocking devices. When embedded PLL is enabled, the clocking reference is automatically calculated using the following equation.

\[
\text{Tile Clock Input} = \frac{\text{Reference Divider \( R \)}}{\text{Reference Divider \( R \)}}
\]

- **Tile Clock Input:** When embedded PLL is enabled, this frequency is the reference frequency of the embedded PLL. When embedded PLL is bypassed, this frequency is the sampling frequency of this tile.

- **Desired Fs:** The sampling frequency generated by the embedded PLL. Configure the desired sampling frequency either directly from an external clocking device, or from the embedded PLL based on the actual hardware design.
Generating a Signal

1. Select the desired channel and Click **Generation**.

2. Select the frequency tone and the number of samples.

3. Click **Generate**.
Acquiring a Signal

1. Select the desired channel and Click **Acquisition**.

2. Select the number of samples and click **Acquire**.
ZCU111 and ZCU1275 Setup

Clock Programming - SCUI

External clocks can be programmed with the System Controller GUI (SCUI) application.

- For the ZCU1275, the SCUI can be found at: https://www.xilinx.com/products/boards-and-kits/zcu1275.html#documentation.
- For the ZCU111, the SCUI can be found at: https://www.xilinx.com/products/boards-and-kits/zcu111.html#documentation.

Setting up the ZCU111 Board

1. Connect the JTAG cable.
2. Connect DAC 229 Tile 1 Channel 3 to ADC 224 Tile 0 Channel 0
   - An optional filter can be used
3. Generate/Acquire waveforms as described in Generating a Signal and Acquiring a Signal.
   - With this connection in place (as shown in the following image), DAC tile 1, channel 3 is connected to ADC tile 0, channel 0
4. For more information, see: https://www.xilinx.com/products/boards-and-kits/zcu111.html#overview

Related Information
Generating a Signal
Acquiring a Signal
### Setting Up the GUI

1. Set up the DAC Tile tab as shown:

![DAC Tile 1 diagram]

2. Set up the ADC Tile tab as shown:

![ADC Tile 0 diagram]
Setting Up the ZCU1275 Board

1. Connect the bullseyes cable to the clock module output.
   - Bullseye 19/20 and 1/2 connect to ADC/DAC clocks
2. Connect the DAC/ADC bullseyes together through DC blocks.
3. Generate/Acquire waveforms as described in Generating a Signal and Acquiring a Signal.
   - Connector 17/18 match DAC/ADC Tile 0 or 2, Channel 0
   - Connector 15/16 match DAC/ADC Tile 0 or 2, Channel 1
4. For more information, see: https://www.xilinx.com/products/boards-and-kits/zcu1275.html#overview
Related Information
Generating a Signal
Acquiring a Signal

Bitstream Generation

This section describes the steps required for customizing the Zynq UltraScale+ RFSoC RF Data Converter IP for a custom board and generating the bitstream of the IP example design. More detailed information for various RF Data Converter IP settings can be found in the Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269).

Creating a Vivado Project

1. Open the Vivado Design Suite.

2. Click Create Project.
3. Click Next.
4. Enter project name and location.
5. Click Next.

6. Select RTL Project.

7. Click Next.

8. Use the filters to find your device.
9. Select the device.
10. Click Next and then Finish.

Adding and Customizing the RF Data Converter IP

1. Click IP Catalog.

2. Find the RF Data Converter IP (you can use the search field to search for it).
3. Double-click the IP.
4. Configure the IP as per your board requirement.
5. Be aware of limitations (see Answer Record AR71746).

6. To speed up the configuration, Predefined Configuration or Simple setup can be used.

**Generating the RF Data Converter IP Example Design**

1. In the Advanced mode tab, enable the RF Analyzer.
2. Click **OK**.

3. You can skip the IP generation on the next screen.

4. In the Source window, select the IP.

5. Right-click and select **Open IP Example Design**.

6. Select the path where the example project will be created.

7. Click **OK**.

**Generating the Bitstream**

1. The example project creates an IP integrator design.

   ![Diagram of an IP integrator design]

   **Note:** You might have to zoom fit to see the full IP integrator design.

2. Click **Generate Bitstream**.

3. When generated, locate the bitstream at `<example_design_path>\ip_name\ip_name.runs\impl_1`. 
Customization and Testing

Customize Clock Frequencies

This evaluation tool GUI provides an easy and flexible mechanism to customize sampling frequency, PL frequency, and sysref frequency. There is one clock generator (LMK04208) and three RFPLLs (LMX2594) onboard that generate the clock for converter tiles, PL clock, and sysref signals. All four of these onboard clock chips are programmable. For details, refer to the ZCU111 Evaluation Board User Guide (UG1271).

To program these clocks chips, load the .tcs file in the Clock Settings tab under Advanced, and click Apply. You can choose to use the .tcs files shipped with this software located under \Data\Clocking\, or you can generate your own configuration with the TICS Pro software and then place it under \Clocking\. For additional information, see Texas Instruments Clocks and Synthesizers (TICS) Pro Software.

In this example, RF-ADC and RF-DAC are clocked directly by an external PLL by using the LMK04208_3932M16.tcs file from under \Data\Clocking\. This file is shipped with this evaluation tool GUI and it retains the default configuration of LMK04208.

LVM and TDMS File Format

LabVIEW Measurement (.lvm) is a text based file format. TDM Streaming (.tdms) is a stream based file format. For testing the Zynq® UltraScale+™ RFSoC with this evaluation software, Xilinx recommends the LVM file format.

LVM File Format

The LabVIEW Measurement (.lvm) file is a native, text based file format of the LabVIEW software. This file format is used in this evaluation tool GUI for data input and output. The .lvm file contains a file header and column based data. Some items in the file header are required. An example .lvm file with the headers required by this evaluation tool GUI is shown in the following figure.
Figure 23: **LVM File Format**

<table>
<thead>
<tr>
<th>LabVIEW Measurement</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Writer_Version</td>
<td>2</td>
</tr>
<tr>
<td>Reader_Version</td>
<td>2</td>
</tr>
<tr>
<td>Separator</td>
<td>Tab</td>
</tr>
<tr>
<td>Decimal_Separator</td>
<td>.</td>
</tr>
<tr>
<td>Multi_Headings</td>
<td>No</td>
</tr>
<tr>
<td>X_Columns</td>
<td>No</td>
</tr>
<tr>
<td>Time_Pref</td>
<td>Relative</td>
</tr>
<tr>
<td>Operator</td>
<td>xlnx</td>
</tr>
<tr>
<td>Date</td>
<td>4/25/2018</td>
</tr>
<tr>
<td>Time</td>
<td>36:46.7</td>
</tr>
<tr>
<td><em><strong>End_of_Header</strong></em></td>
<td></td>
</tr>
<tr>
<td><em><strong>Start_Special</strong></em></td>
<td></td>
</tr>
<tr>
<td>Version</td>
<td>V1.0.0 Beta2</td>
</tr>
<tr>
<td>Fs(MHz)</td>
<td>2000</td>
</tr>
<tr>
<td><em><strong>End_Special</strong></em></td>
<td></td>
</tr>
</tbody>
</table>

| Channels | 2 |
| Samples  | 4 |
| Date     | 4/25/2018 |
| Time     | 36:46.7 |
| X_Dimension | Time |
| X0       | 0 |
| Delta_X  | 5.00E-10 |
| ***End_of_Header*** |  |

<table>
<thead>
<tr>
<th>X_Value</th>
<th>I vector</th>
<th>Q_vector</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>9298</td>
<td></td>
<td>-6573</td>
<td></td>
</tr>
<tr>
<td>11280</td>
<td></td>
<td>-6</td>
<td></td>
</tr>
<tr>
<td>9133</td>
<td></td>
<td>6436</td>
<td></td>
</tr>
<tr>
<td>3720</td>
<td></td>
<td>10422</td>
<td></td>
</tr>
</tbody>
</table>

For more information about the `.lvm` file format, see LabVIEW Measurement Files.
TDMS File Format

The TDMS file format targets the management and exchange of large and complex data sets. Unlike the text-based lvm format, the TDMS file is stream-based and thus, more difficult to generate and difficult to view in a simple text editor. National Instruments (NI) provides different tools such as a function library in MATLAB® and C/C++ that work with the TDMS file. NI also provides Excel add-ins for the TDMS file. The following figure shows a TDMS file open in Excel using the TDM Excel add-in.

![Figure 24: TDMS File Format](image)

For additional details, see The NI TDMS File Format.

Loopback Test Example

This section provides an example for running a loopback test. In this example, you can see functions that include customizing the clock, data input and output, and building the .lvm file.

Customize Clock and Data Pattern

The following steps show how to build the onboard clock files and test vector that are required for the loopback test.
1. Build the clock configuration file. Clock the RF-ADC and RF-DAC with 3932.16 MHz from directly onboard the RFPLL. Keep the reference of RFPLL at 122.88 MHz, which means you only need to build the configuration file for LMX2594. This can be done by changing the output from 245.76 MHz to 3932.16 MHz. Choose the \\Data\Clocking\LM2594_3932M16.tcs file or generate it with TICS Pro Software and then save it under \\Data\Clocking.\.

2. Build the test vector for RF-DAC. Build the test vector of a single tone at 240 MHz. This frequency is an integer multiple of the FFT resolution when the sampling frequency is at 3932.16 MHz and the sampling number is 8192. Generate this test vector using an application such as MATLAB®, Python, or Excel. Attach the header of the lvm file, save it under \Data\DAC\. The beginning and end of the t111.lvm file is shown in the following figure.

```
LabVIEW Measurement
Writer_Version 2
Reader_Version 2
SeparatorTab
Decimal_Separator .
Multi_Headings No
X_Columns No
Time_Pref Relative
Operator xlnx
Date 5/15/2018
Time 36:46.7
***End_of_Header***
***Start_Special***
Version V1.0.0 Beta2
Fs(MHz) 3932.16
***End_Special***

Channels 1
Samples 8192
Date 5/15/2018
Time 36:46.7
X_Dimension Time
X0 0
Delta_X 2.54E-10
***End_of_Header***
X_Value I_vector
0
12015
22285
29318
32091
```
Test Steps

1. Connect a pair of single-ended RF-ADC and RF-DAC ports using an SMA cable. AC-coupling capacitors are present on the signal chain. Connecting differential ports is also acceptable, however, a DC blocker is required on both the P and N connectors.

2. Open the evaluation software by clicking Clocking → Advanced in the overview page. Select the configuration file, 122.88 MHz output for LMK04208 and 3932.16 MHz output for LMX2594 (just built), then click Apply.

3. Configure PLL in the RF-ADC and RF-DAC tiles, bypass internal PLL, and enter 122.88 MHz as the reference frequency for reference spur analysis in the FFT page.

4. Configure the RF-DAC and RF-ADC with real-to-real mode. The reference frequency of 240 MHz is not high and hence a 2× decimation factor can be selected for the RF-ADC (this does not adversely affect other configurations).

5. In the RF-DAC FFT page, select From File in the Signal Type box, then click File. All the lvm files (assuming that the lvm file format has been selected in Settings → Data File Format) under \Data\DAC\ are shown in the drop down list. Select the one you plan to test. The file is loaded into memory and the FFT plot is displayed on the left. Click Generate to output the data. After this evaluation tool GUI has run, click the reload icon beside the file box if you placed your file under the \Data\DAC\ folder.
6. Because the RF-DAC is looped back to the RF-ADC, this signal can be captured in the corresponding RF-ADC channel.

7. To export data, as previously described, click File → Export ADC Data, and save the raw data under \Data\ADC\ with the lvm file. You can also select Time Domain, right-click on the plot area, choose Export → Export Data To Clipboard, and then paste it in a text editor.
8. After the raw data is saved to a file, it can be analyzed with FFT tools. See the example plot in the following figure.
FFT Metrics

There are many converter metrics on the RF-ADC FFT page. These metrics are listed and defined as follows.

Figure 25: RF-ADC FFT Metrics

- **dBFS**: dBFS is the full scale of the RF-ADC expressed in dB, normalized to 0. The dBm value of 0 dBFS depends on the input impedance of the RF-ADC (100 Ω for Zynq® UltraScale+™ RFSoC) and acceptable full scale input level (Vppd = 1V), for Zynq UltraScale+ RFSoC, 0 dBFS is 1 dBm.

- **FundA**: RMS power level of fund signal expressed in dBFS.

- **SFDR**: Spurious-free dynamic range (SFDR) expressed in dBc. SFDR is the ratio of the RMS value of the signal to the RMS value of the peak spurious spectral component for the analog input that produces the worst result.

- **SFDRxH23**: SFDR excludes the second and third harmonic distortion in dBc. The location of harmonic distortions are predictable and hence can be handled separately in application. Therefore, a separate SFDRxH23 is listed for reference.

- **Fspur**: The frequency location of the worst spur in MHz in the first Nyquist band.

- **FspurxH23**: The frequency location of the worst spur excludes the second and third harmonic distortion in MHz in the first Nyquist band.
- **THD**: Total harmonic distortion (THD) in dBc. THD is the ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.

- **NSD**: Noise spectrum density (NSD) in dBFS/Hz. NSD is the RMS noise power per Hz normalized to full scale in the first Nyquist band. The noise power in this software indicates total other power except the power of the found signal.

- **SNR**: Signal to noise ratio (SNR) in dB. SNR is the ratio of the RMS signal amplitude to the RMS value of the sum of all the spectral components except the first six harmonics and dc. The unit in dBFS indicates the signal here and refers to full scale of RF-ADC.

- **SNDR**: Signal to noise and distortion ratio (SNDR) expressed in dBc. SNDR is the ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except fund signal. It is similar to SNR, but includes all the harmonics.

- **IM3**: Third-order inter-modulation (IM3) distortion products expressed in dBc. IM3 used in dual-tone testing, indicates the ratio of RMS signal amplitude to the maximum RMS amplitude of $2F_2 \pm F_1$ or $2F_1 \pm F_2$.

- **F\text{ref} Spurs**: Spurs generated by the input reference (the frequency of phase-frequency-detector) of the PLL, including its harmonics. When using an external PLL for clocking the Zynq UltraScale+ RFSoC directly, you must indicate the reference frequency in the PLL tab for this evaluation tool GUI to calculate the $F\text{ref}$ spurs. The RF-ADC is built with interleaving technology. Spurs of offset interleaving and gain/timing interleaving are listed on the RF-ADC FFT tab by choosing Interleaving Performances.

- **Interleave Offset**: The frequency location and amplitude of offset interleaving spurs.

- **Interleave Gain**: The frequency location and amplitude of gain/timing interleaving spurs.

---

**Appending Files**

**RF-DAC Data Pattern**

Data patterns with the TDMS or LVM file format are available for reference under `\Data\DAC\`. The contents of these files can be easily identified from the file name. Here is an example of a file name, `IQ_1x_QAM256_RRC0.1_50M_BB491.52MHz_length_16M_-15dB.tdms`.

This file name means that the data pattern is in IQ (complex) format, there is one QAM256 modulated carrier, the RRC roll-off coefficient is 0.1, carrier bandwidth is 50 MHz, data sampling rate is 491.52 MHz, data length is around 16M samples, carrier amplitude is ~15 dBFS, and the file format is TDMS. Configure RF-DAC in IQ mode at the digital side, set the RF-DAC sampling clock at 3932.16 MSPS, set the interpolation factor as 8 ($491.52M \times 8 = 3932.16$ MHz), then load this file from the RF-DAC FFT page, and you will see the correct carrier.
Note: The maximum number of samples that the BRAM can handle is 32K for IQ data and 64K for real data. Switch to the DDR mode (in Memory Type) for data sources if the number of samples is greater than this limitation.

The following figure illustrates the FFT plot of this carrier captured by RF-ADC with a loopback path. In this example, the RF-DAC is set in 32 mA/3V mode and some digital gain to increase carrier amplitude seen by the RF-ADC.

Figure 26: RF-DAC Test Pattern Example

Configuration and Preferences

Configurations (.cfg) and preferences (.prf) are available under \Config\. Configurations and preferences are provided in pairs for easy evaluation. The major properties can be found from file name, for example, RFDC_Example_BRAM_ADC_DAC_8X8_Loop_C2R_X8_3932P16M.cfg. This configuration sets sampling frequencies of 3932.16 MHz for all eight RF-ADCs and RF-DACs with decimation and interpolation of 8× and the BRAM selected.
Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select Help → Documentation and Tutorials.
- On Windows, select Start → All Programs → Xilinx Design Tools → DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:
Appendix B: Additional Resources and Legal Notices

1. ZCU111 Evaluation Board User Guide (UG1271)
3. LabVIEW Run-Time Engine 2017 SP1
4. Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269)
5. Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926)
6. ZCU111 System Controller – GUI Tutorial (XTP517)
7. Texas Instruments Clocks and Synthesizers (TICS) Pro Software
8. LabVIEW Measurement Files
9. The NI TDMS File Format

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