WP172 (v1.0) January 15, 2003

# *Spartan-IIE FPGAs Lower I/O Cost*

*By: Ashok Chotai*

Today's designers are faced with the need for lower cost and an increased number of I/Os. This white paper will show you how the Spartan™-IIE Family addresses these needs. The Spartan-IIE family has been specifically designed for consumer designs with a heavy focus on total system cost. When you are considering designing with an FPGA, the Spartan-IIE family is the obvious choice delivering the most I/O for your money. Additionally, the Spartan-IIE offers a hassle free density migration path and a highly efficient I/O banking scheme, with substantial I/O standards to further reduce your system cost.

## Highest I/O Counts

Higher system bandwidth and wider I/O bus standards such as 64-bit, 66 MHz PCI demand more I/Os for today's consumer designs. The Spartan-IIE family addresses these needs by providing up to 514 I/Os (see Table 1) and up to 400 Mb/s LVDS performance. There is no other low cost FPGA family that can provide you with the performance and amount of I/O as the Spartan-IIE family.

## Flexible Density Migration

You have the ability with Spartan-IIE to easily enhance your product with a density migration path that gives you increased I/O without requiring a board re-spin or footprint change (see Figure 1). You, as a designer often select one particular density device when the design starts, but end up using either a smaller or a larger density. This change could be due to any of these reasons — different features needed, change in marketing requirements, last minute enhancements, or cost reduction. The Spartan-IIE family addresses this need by offering you density migration capability within the family (see Table 1).

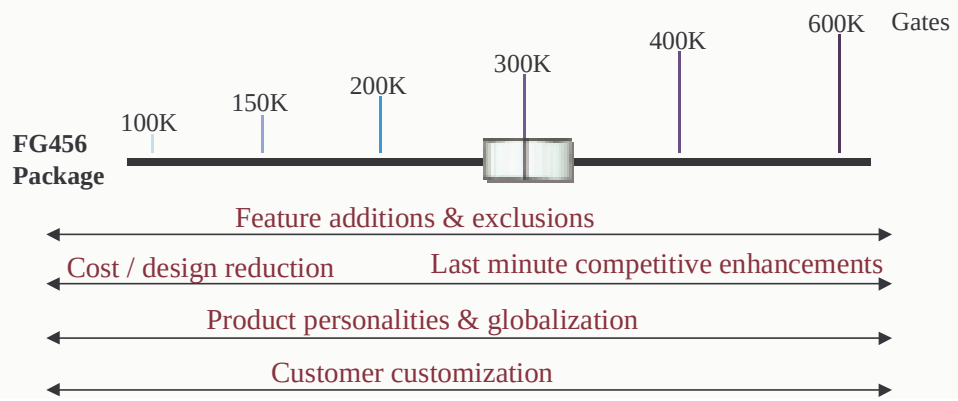


*Figure 1:* **Need for Density Migration**

*Table 1:* **Device Migration Across Spartan-IIE Devices**

| | Available User I/O | | | | |
|---|---|---|---|---|---|
| Device | TQ144 | PQ208 | FT256 | FG456 | FG676 |
| XC2S50E | 102 | 146 | 182 | - | - |
| XC2S100E | 102 | 146 | 182 | 202 | - |
| XC2S150E | - | 146 | 182 | 265 | - |
| XC2S200E | - | 146 | 182 | 289 | - |
| XC2S300E | - | 146 | 182 | 329 | - |
| XC2S400E | - | - | 182 | 329 | 410 |
| XC2S600E | - | - | - | 329 | 514 |

| Density Migration | |
|---|---|
| TQ144 | 2 devices |
| PQ208 | 5 devices |
| FT256 | 6 devices |
| FG456 | 6 devices |
| FG676 | 2 devices |

# More I/O Banks and I/O Standards

## I/O Banks

The Spartan-IIE family has up to eight I/O banks. Each I/O bank is individually programmable to support any of 19 I/O standards, including three differential I/O standards. Some of the I/O standards require I/O voltage ($V_{CCO}$) and/or independent reference voltage ($V_{REF}$). You can connect multiple components simultaneously with various I/O types as long these standards use the same $V_{CCO}$ voltage and have the same $V_{REF}$ voltage (always not needed) within a bank. This gives you twice as much flexibility and banking capability relative to other low cost FPGAs.

## I/O standards

The Spartan-IIE family provides programmable I/O pins that support 19 commonly used I/O standards. These standards include 16 single-ended standards and three differential standards. The I/O standards allow a single FPGA to directly interface with backplanes, memories, microprocessors, and other devices. Direct interface eliminates the need for external converters or translators, improving the critical chip-to-chip speed and simplifing system board design as well as reducing your system cost (see Table 2).

Spartan-IIE devices support multiple high-speed differential I/O standards including LVDS, Bus LVDS and LVPECL. These differential standards facilitate higher data transfer rates, lower power consumption, lower electromagnetic interference (EMI), higher noise immunity and simplified printed circuit board design which are becoming more widely used in consumer applications.

*Table 2:* **Spartan-IIE I/O Standards and Typical Applications**

| Standard | Application |
|---|---|
| LVTTL | Chip-to-chip, Memory |
| LVCMOS/2.5/1.8 | Chip-to-chip |
| PCI 3.3V - 32/64 bit, 33MHz | PC, Embedded systems |
| PCI 3.3V - 32/64 bit, 66MHz | PC, Embedded systems |
| SSTL2 Class I & II | DDR SDRAM |
| SSTL3 Class I & II | SDRAM |
| HSTL Class I, III & IV | QDR SRAM, Cache RAM, SRAM, CSIX |
| GTL | Backplane, Processors |
| GTL+ | Backplane, Processors |
| CTT | Backplane, Memory |
| AGP | Graphic processors |
| LVDS (Clock & Data) | Chip-to-chip |
| Bus LVDS | Chip-to-chip |
| LVPECL | Clock |

## Programmable Drive Strength

The Spartan-IIE I/O structure supports output current drive strengths of 2, 4, 6, 8, 12, 16, and 24 mA. These drive strengths are user configurable and can be varied depending on the requirements of the application. These programmable drive-strength settings help you decrease the effects of simultaneously switching outputs (SSO), reduce system noise, decrease power consumption, and improve signal integrity.

## Conclusion

The Spartan-IIE family addresses the need of today's challenging times with the best I/O counts, consumer functionality, and the lowest cost per I/O. You get a proven architecture and density migration path for reduced risk. The system level features combined with output drive strength provide you with high-performance and cost-effective system integration. The Spartan-IIE family offers system level features such as on-chip distributed RAM and block RAM, 19 I/O standards including three differential standards, and four DLLs for clock management (see Table 3). For more information on Spartan-IIE family, please visit our website at http://www.xilinx.com/spartan2e.

*Table 3:* **Spartan-IIE Family Product Matrix**

| Device | XC2S50E | XC2S100E | XC2S150E | XC2S200E | XC2S300E | XC2S400E | XC2S600E |
|---|---|---|---|---|---|---|---|
| System Gates | 50K | 100K | 150K | 200K | 300K | 400K | 600K |
| Logic Cells | 1,728 | 2,700 | 3,888 | 5,292 | 6,912 | 10,800 | 15,552 |
| Block RAM Bits | 32K | 40K | 48K | 56K | 64K | 160K | 288K |
| DLLs | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| I/O Standards | 19 | 19 | 19 | 19 | 19 | 19 | 19 |
| Max Differential I/O Pairs | 83 | 86 | 114 | 120 | 120 | 172 | 205 |
| Max Single Ended I/O | 182 | 202 | 265 | 289 | 329 | 410 | 514 |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 01/15/03 | 1.0 | Initial Xilinx release. |