WP208 (v1.1) January 14, 2004

Flip-Chip Package Substrate Solder Issue

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Alpha particle emission in close proximity to the device circuitry is minimized by following Xilinx low alpha solder requirements on package substrate pads. One flip-chip packaging vendor's failure to comply with these requirements has resulted in contamination by high alpha solder causing possible soft errors due to flipped device configuration bits. This white paper provides an overview on soldering material, describes the specific soldering problem, and offers some solutions.

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Background

Xilinx flip-chip packages are assembled using a solder bump interconnection process. Figure 1a shows the cross section of a flip-chip package. The active side of the silicon die contains an area array of pads on which solder bumps are attached. The package substrate pads also contain solder paste (presolder or SOP) that melts during assembly to form the solder bump interconnection, as shown in Figure 1b and Figure 1c.

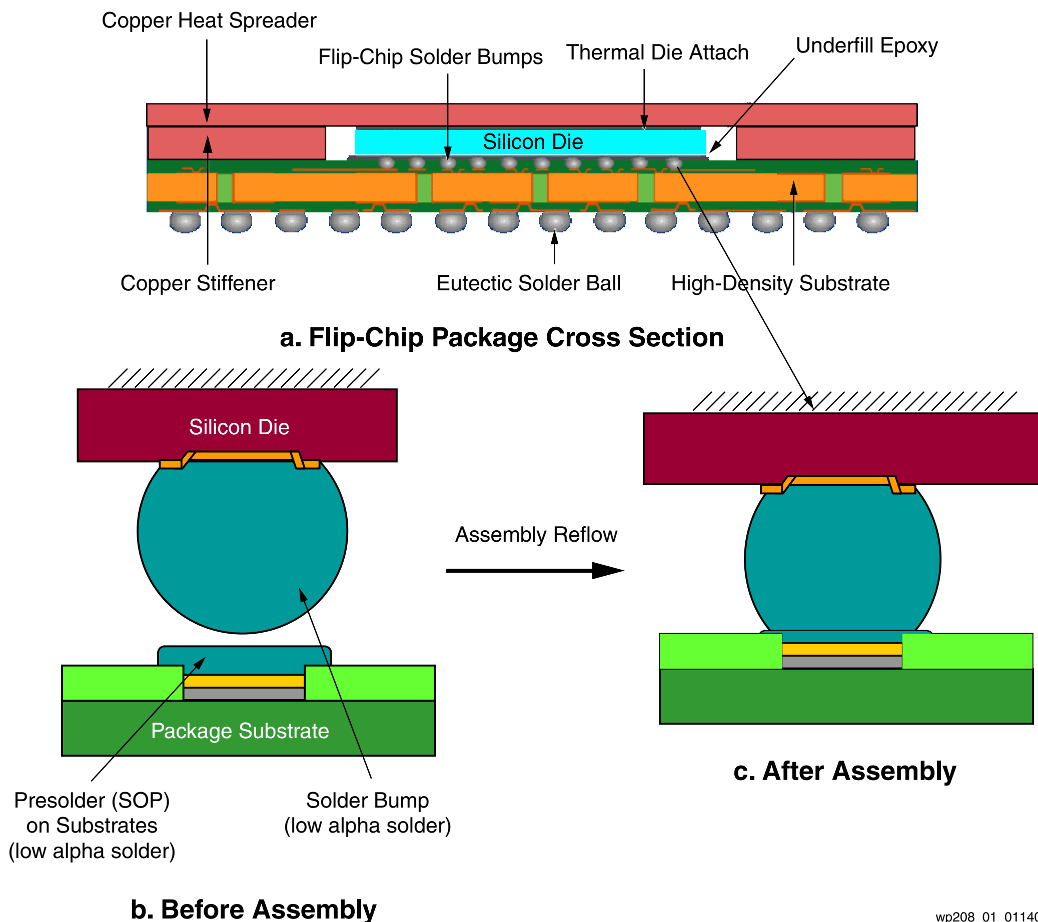

Figure 1: **Solder Bump Interconnection within Flip-Chip Packages**

Xilinx requires that all flip-chip bumping and substrate vendors use low alpha solder to minimize the alpha particle emission in close proximity to the device circuitry.

Description of the Issue

Xilinx recently determined that one package substrate vendor was not in compliance with our low alpha solder requirements on package substrate pads. As a result, the solder bump interconnections on some of these devices were contaminated by small amounts of high alpha solder. The increased rate of alpha particle emission from the bumps can cause a configuration bit to be “flipped” to its opposite state (“flipped bits”) causing soft errors. Based on recent data, we anticipate one flipped bit per device at the rate of once every 230 to 2500 hours of continuous operation, depending on the device. The bit flip rate for this issue is proportional to the number of solder bumps directly over configuration memory cells. It also is dependent on the alpha particle emission rate of the solder, which can vary by a factor of 10. The estimated bit

flip mean-time between failure (MTBF) values for the affected devices are listed in Table 1.

Table 1: **Estimated Bit Flip Mean Time Between Failure**

Device	Estimated Bit Flip MTBF (Days)
2VP2	246
2VP4	132
2VP7	100
2VP30	37
2VP40	25
2VP50	24
2VP70	19
2VP100	14
2V6000	26

The effect of the bit flip rate on the design failure rate is highly design dependent and can vary dramatically. For example, the number and location of configuration bits used varies significantly with each design. Bit flips are random events that can happen at any time, and there is a finite probability that any bit flip can cause a design failure. The longer a device is operational, the higher the probability that more bits will flip, and the higher the probability of a design failure.

Regarding functional failures, the MTBF was evaluated for a limited number of designs. Functional MTBF values were observed as low as five times and as high as 50 times the bit flip MTBF. Table 2 shows estimated design MTBF values for various ratios of bit flip to design MTBF.

Table 2: **Estimated Functional MTBF Values for Different Ratios of Functional to Bit Flip MTBF**

Device	5:1 Design MTBF (Years)	10:1 Design MTBF (Years)	50:1 Design MTBF (Years)
2VP2	3.4	6.7	33.7
2VP4	1.8	3.6	18.1
2VP7	1.4	2.7	13.7
2VP30	0.5	1.0	5.1
2VP40	0.3	0.7	3.4
2VP50	0.3	0.7	3.3
2VP70	0.3	0.5	2.6
2VP100	0.2	0.4	1.9
2V6000	0.4	0.7	3.6

Recommendations

Xilinx recommends that customers return the affected production material by the normal RMA process via Xilinx sales representatives.

Applications with non-continuous device operation, such as prototyping, might be less sensitive to configuration bit changes. Smaller devices are less likely to experience bit changes than larger devices.

Please contact your Xilinx FAE for more information.

Corrective Action

This soldering issue has been resolved and does not affect device and package combinations assembled from January 1, 2004 (date code 0401) and later.

Appendix: Brief Introduction of Soft Error

The solder paste used for assembly of electronic packages is made up of lead-based alloys. Any naturally mined Pb has several isotopes that undergo radioactive decay over time. The decay process generates new isotopes and resulting energetic particles, such as ionized alpha particles. Thus, standard solder paste used in the industry is uncontrolled for alpha emitting isotopes. The alpha emission rate could be as high as 10 to 100 counts per hour per square centimeter (CPH/cm^2). An alpha particle from standard lead solder has an energy spectrum from kilo-electron volts to up to 5 million electron-volts (MeV). Such alpha particles can penetrate silicon only for a fraction of a millimeter (mm). For sensitive electronic applications where Pb is used in close proximity to the circuit, these materials are refined to reduce alpha-emitting isotopes. These low-emission solder materials are called low alpha solder.

When an ionized particle interacts with a semiconductor, electron-hole pairs are generated along the path of the incident particle. These generated electron-hole pairs can be transported through the semiconductor by drift and diffusion processes, which ultimately can generate transient device currents. Under certain biasing conditions the transient currents can alter the previously stored state of the circuit, causing an error in the data stored in the circuit. This phenomenon generally is referred to as a *soft error.*

In memory devices, the soft error has two attributes:

1. The data read from a location differs from the data originally written to that location.
2. There is no physical damage or degradation to the memory, which continues to function normally thereafter.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/09/04	1.0	Initial Xilinx release.
01/14/04	1.1	Inserted minor changes and additional clarification.