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Achieving Higher System Performance with the Virtex-5 Family of FPGAs

By: Adrian Cosoroaba and Frédéric Rivoallon

The Virtex™-5 devices comprise a multi-platform FPGA family based on second-generation Advanced Silicon Modular Block (ASMBL™) column-based architecture. With several new architectural elements designed for maximum performance, higher integration, and lower power consumption, Virtex-5 devices attain higher levels of system performance than previously possible.

Maximum system performance requires a balanced mix of performance-efficient FPGA components: logic fabric, on-chip RAM, DSP blocks, and I/Os. This document shows the level of performance that can be reached with Virtex-5 family building blocks, with particular emphasis on the new ExpressFabric™ technology. The main features of this new technology, including the new 6-input LUT, are described in this paper. Examples that quantify the performance improvements for logic and arithmetic functions are presented along with other enhancements for on-chip RAM, DSP blocks, and I/Os.

Performance with Margin to Spare

Performance benchmarks based on customer designs show that the Virtex-5 family ExpressFabric technology provides an average 30% improvement in performance over previous-generation Virtex-4 devices — the equivalent of about two speed grades.

The Virtex-5 family is the platform of choice for high-performance designs; its logic fabric and hard IP blocks can operate at 550 MHz clock rates. For example, many functions in the logic fabric, such as counters, adders, and storage (RAM/ROM) implemented with LUTs, are capable of performing at that clock rate. The hard-IP blocks — memory and DSP — have also been designed to operate at the same speed.

ExpressFabric Technology

The new ExpressFabric technology is based on a 6-input LUT architecture and routing that uses diagonally symmetric interconnect patterns.

6-Input LUT Architecture

The combination of look-up tables (LUTs), special functions like carry chains and dedicated multiplexers, and flip-flops (FFs), together with the methods by which these elements are connected, determines the performance and efficiency of implementing logic and arithmetic functions.

The Virtex-5 family ExpressFabric technology is an evolutionary step, building on the experience that Xilinx has gained over the years. Since the first FPGA was introduced and produced in the mid-1980s, most FPGAs have been based on the same fundamental architecture: the 4-input LUT. The one thing all previous FPGAs had in common is that functions requiring more than four inputs had to be implemented using a combination of several LUTs and/or multiplexers.

The Virtex-5 family is the first FPGA platform to offer a real 6-input LUT with fully independent (not shared) inputs. This leads to some very compelling advantages.

In order to increase logic fabric performance, it is essential to minimize the critical path delay through the LUTs. The LUT input architecture is the determining factor. At 65 nm, the 6-input LUT provides the right trade-off between critical path delay and design die size, as illustrated in Figure 1.

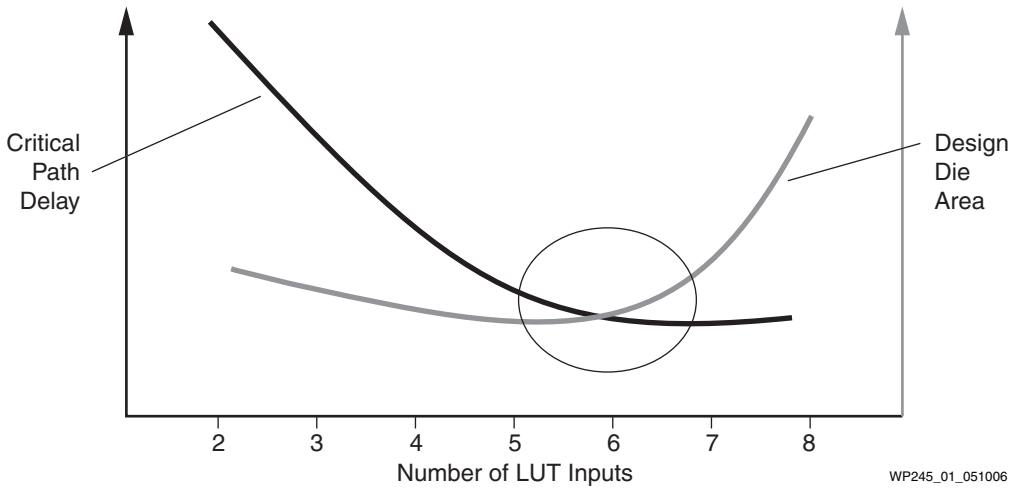


Figure 1: **Making the Right Trade-off for LUT Input Architecture at 65 nm**

With a wider LUT input, critical path delay decreases but reaches a point of diminishing returns for LUTs with more than six inputs. On the other hand, the design die size also increases for LUTs with more than six inputs due to the inefficient use of the wider-input LUTs.

The Virtex-5 family introduces some additional differences in its logic architecture. Table 1 gives an overview of the differences between the Virtex-4 and Virtex-5 family Configurable Logic Blocks (CLBs).

Table 1: **Virtex-4 / Virtex-5 CLB Logic Resources Comparison**

CLB	Virtex-4 FPGA	Virtex-5 FPGA
Slices	4	2
LUTs	8	8
Flip-Flops	8	8
Clocks, Clock-Enables, Resets	4 each	2 each
Distributed RAM	64 bits	256 bits
Shift Register Length	64 bits	128 bits
Multiplexers	16 – 1	2 x (16 – 1)

To better understand the changes introduced with the new Virtex-5 family architecture, the Virtex-4 architecture must be briefly summarized.

The basic Virtex-4 family logic element is composed of a 4-input LUT and a flip-flop, and additional elements such as a function expander and an arithmetic cell. The function expander enables larger LUT structures (such as 5-input or 6-input LUTs) to be built. In RAM mode, the Virtex-4 LUT can implement a 16-bit memory element, a 16-bit shift register, or even a loadable LUT whose content can be changed during operation. This distributed RAM mode, unique to Xilinx FPGAs, offers very efficient small memories.

As in previous Xilinx FPGA families, the Virtex-5 SLICEL can implement logic functions, registers, and arithmetic functions using the dedicated carry chain. See Figure 2.

The slightly more complex SLICEM adds the capabilities of implementing distributed RAM and shift registers (SRLs) with LUTs.

The new 6-input LUT has a second output that can be used to initialize the carry chain or change the 6-input LUT into two 5-input LUTs with common inputs. See Figure 3.

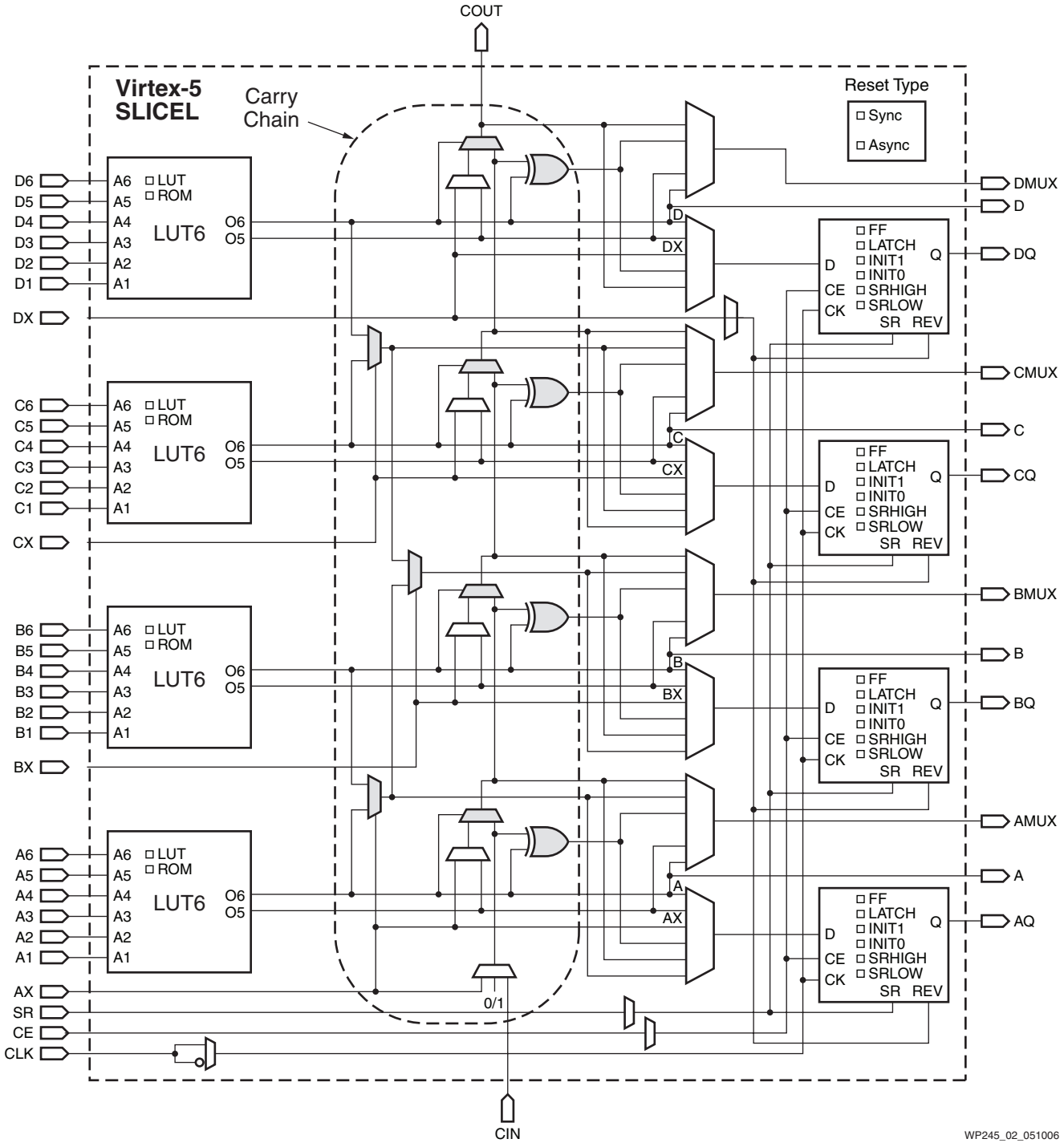


Figure 2: **Block Diagram of Virtex-5 SLICEL**

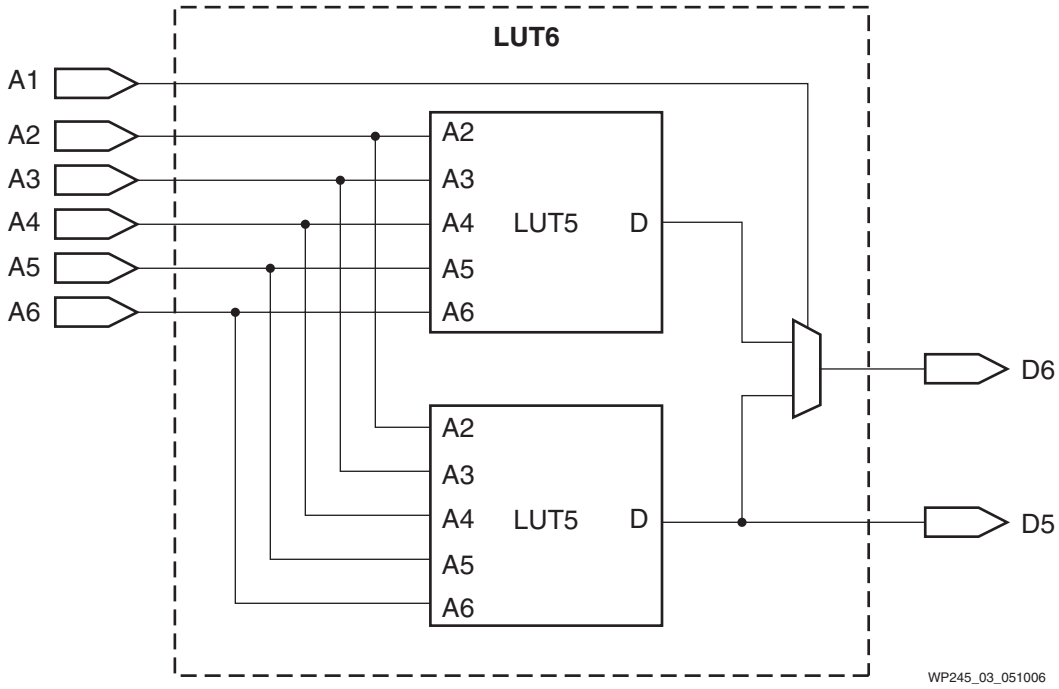


Figure 3: **Block Diagram of a Virtex-5 6-Input LUT**

The 6-input LUT leads to several benefits:

- As it implements wider functions directly in the LUT, the number of logic levels between registers is reduced, leading to higher performance.
- It implements significantly more logic than a LUT with four inputs.
- Power consumption is reduced because the larger LUT reduces the amount of required interconnect (routing resources).

The Virtex-5 family SLICEM LUTs also provide additional benefits:

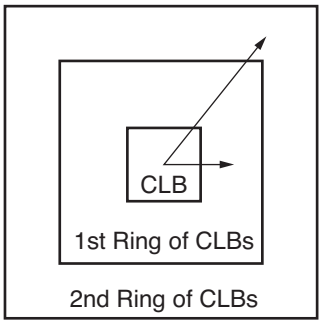
- *New aspect ratios for distributed RAM*. Every LUT can be configured as a 64 x 1 or 32 x 2 distributed RAM. Benefits for the designer are a much denser and faster implementation of distributed RAM with increased flexibility.
- *Longer SRL chains*. A single LUT supports a 32-bit SRL. A slice can thus implement a shift register of up to 128 bits, providing significant area savings and reduced routing resources in comparison to previous architectures. Shift registers are features available only in Xilinx devices. The Xilinx ISE™ software packer automatically packs two 16-bit SRLs with common addressing but different data. In other words, if the application needs a 16-bit deep, 8-bit-wide shift register, it can be implemented in a single slice.

Routing and Interconnect Architecture

With process technology advancements, interconnect timing delays can account for more than 50% of the critical path delay. A new diagonally symmetric interconnect pattern, developed for the Virtex-5 family, enhances performance by reaching more places in fewer hops. The new pattern allows for more logic connections to be made within two or three hops. Moreover, the more regular routing pattern makes it easier for the Xilinx ISE software to find the most optimal routes. All of the interconnect features are transparent to FPGA designers, but translate to higher overall

performance and easier design routability. Essentially, the Virtex-5 family interconnect pattern provides fast, predictable routing based on distance.

Figure 4 compares the delays incurred from a source register in one CLB driving a LUT packed with a second register in a surrounding CLB. The goal is to measure the effect of the incremental routing delays for both the Virtex-4 and Virtex-5 family architectures.



	Virtex-4	Virtex-5
1st Ring	751 ps	665 ps
2nd Ring	906 ps	723 ps

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Figure 4: **Routing Delay Comparison for Virtex-4 and Virtex-5 FPGAs**

Design Examples

The benefits of the new 6-input LUT architecture are detailed in the following examples.

Multiplexers

One of the easiest examples is a multiplexer. A four-input LUT can implement a 2:1 MUX. Every multiplexer that has more than two inputs requires additional logic resources. A 4:1 MUX needs two 4-input LUTs and a MUXF in Virtex-4 architecture. With the new 6-input LUT, this 4:1 MUX is now implemented with a single LUT. An 8:1 MUX in a Virtex-4 device requires four LUTs and three MUXFs. With the new Virtex-5 family architecture, only two 6-input LUTs are required, resulting in better performance and better logic utilization. See Figure 5.

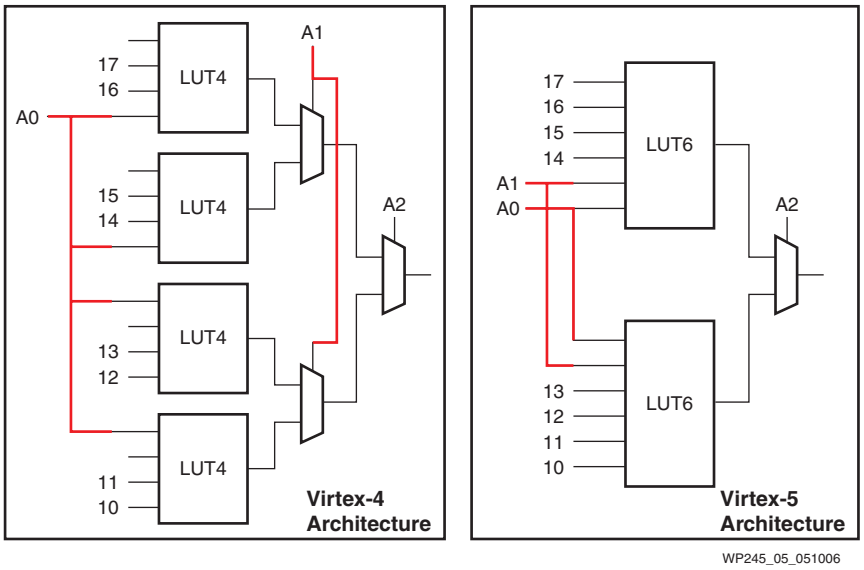

Figure 5: **8:1 MUX Implementation Using Virtex-4 and Virtex-5 Architectures**

Distributed RAM and Shift Registers

Distributed memory functions (LUT RAM) benefit in several ways from the larger LUT. The new aspect ratios allow a much denser packing of small memory functions, leading to significant performance benefits. See Figure 6.

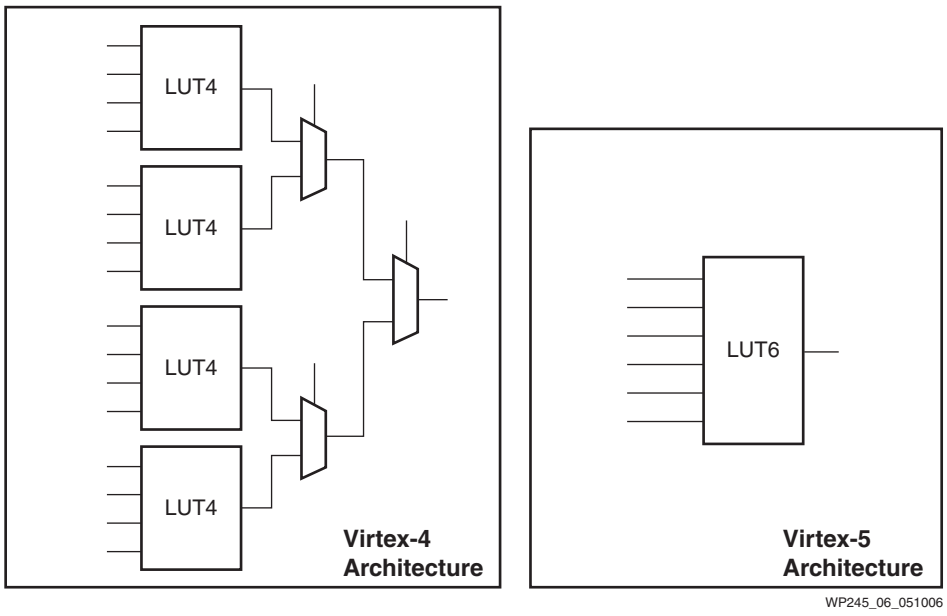

Figure 6: **64-Bit LUT RAM Implementation in Virtex-4 and Virtex-5 FPGAs**

Arithmetic Functions

There are also several improvements in arithmetic functions implemented in the Virtex-5 family architecture:

- Support for ternary adds (using one carry chain)
- Complex carry start logic

- "Free" Ground or V_{CC} to initialize the carry function

The performance for arithmetic functions as measured by the path delay is significantly improved, as shown in Figure 7.

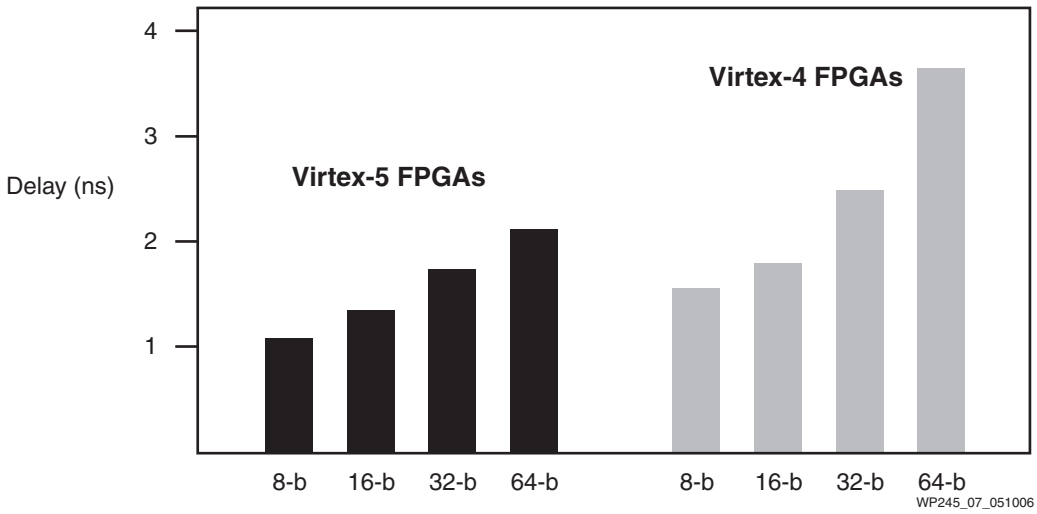

Figure 7: **Multi-Bit Adder Timing Comparison for Virtex-4 and Virtex-5 FPGAs**

Performance Advantages for Functional Blocks

Table 2 shows a performance comparison of logic and arithmetic functions between the Virtex-4 and Virtex-5 families. Figures shown are for the fastest speed grade in each device family. Designs were run through ISE 8.1i software.

Table 2: **Performance Comparisons of Functional Blocks**

	Virtex-4 FPGA	Virtex-5 FPGA
6-Input Function(1)	1.1 ns	0.9 ns
Adder, 64-bit	3.5 ns	2.5 ns
Ternary Adder, 64-bit	4.3 ns	3.0 ns
Barrel Shifter, 32-bit	3.9 ns	2.8 ns
Magnitude Comparator, 48-bit	2.4 ns	1.8 ns
LUT RAM, 128 x 32-bit	1.4 ns	1.1 ns

Notes:

1. Virtex-5 FPGAs use one 6-input LUT and Virtex-4 FPGAs use two 4-input LUTs

Block RAM

The block RAM base size in the Virtex-5 family has increased to 36 Kbits (from 18 Kbits in the Virtex-4 family). This makes it easier to build larger memory arrays in Virtex-5 devices. In addition, the 36 Kb block RAM can be used as two independent 18 Kbit block RAMs, hence, there is essentially no penalty for building many 18 Kbit or smaller RAM arrays on-chip.

The Virtex-5 family block RAM can be operated in Simple Dual Port mode to effectively double the block RAM bandwidth. Simple Dual Port mode allows the

Virtex-5 family block RAM width to be expanded beyond 32 bits up to as much as 72 bits per block RAM.

New or enhanced block RAM features include:

- Integrated 64-bit ECC with optional scrubbing
- Hard-coded synchronous FIFO option
- FIFO support for widths up to 72 bits in a single block
- Dual-port widths up to x36 total
- Simple dual-port widths up to x72
- New power management circuits in the block RAM: Within each 18K block, if 9K or less is used, the other half is automatically turned off (~ 50% reduction)
- Built-in cascade logic which allows adjacent block RAMs to be cascaded together into a 64Kx1 RAM
- Block RAM operates up to 550 MHz, providing an extra level of performance over the 500 MHz Virtex-4 FPGA

DSP

The Virtex-5 family introduces the DSP48E slice, a new DSP slice that provides major enhancements over the DSP48 slice in the Virtex-4 FPGA:

- *Increased multiplier width.* The Virtex-5 DSP48E slice is based on 25 x 18 bit multipliers (versus 18 x 18 in Virtex-4 devices). The increase to 25 x 18 can lead to fewer cascade stages, yielding higher overall performance and utilization.

  One application that uses wider multiplication capability is floating point, which uses 24 x 24 unsigned multipliers for single-precision floating point multiply. A 24 x 24 unsigned multiplier is built with two DSP48E slices, half the number needed with Virtex-4 DSP48 slices. Single-precision floating point support is actually a subset of the 35 x 25 capability available with two DSP48E slices. In Virtex-4 devices, two DSP48 slices creates a 35 x 18 multiplier, while four DSP48 slices creates a 35 x 35 multiplier of which a 24 x 24 unsigned multiplier is a subset.
- *Independent C registers.* In Virtex-5 devices, the number of signals available for the DSP48E slice has increased, allowing for independent C registers. This offers more flexibility and easier implementation of DSP algorithms.
- *Logic Unit Functionality.* In Virtex-5 devices, the adder stage has been expanded to support logic functions. Some of the logic functions supported are bitwise XOR, XNOR, AND, and NOT functions when the first-stage multiplier is bypassed.
- *The DSP48E slice operates up to 550 MHz* providing an extra level of performance over the 500 MHz Virtex-4 FPGA.

Parallel I/O

Getting an FPGA to run fast internally is only part of the battle. Maximum system performance requires high-performance interaction links between the FPGA and the other components of the system.

The SelectIO™ technology in Virtex-5 family contains many of the popular features found in Virtex-4 devices, such as ChipSync™ technology and digitally controlled impedance (DCI) for single-ended and differential support.

Enhancements include:

- *40 I/Os per bank.* This is a reduction from the 64 I/Os per bank in Virtex-4 devices, thereby providing finer granularity.
- *Up to 1,200 user I/Os* with ChipSync technology in every I/O.
- *ODELAY.* In the Virtex-4 family ChipSync logic, programmable IDELAY elements were provided on all inputs in order to facilitate clock-data alignment. In the Virtex-5 family, the block can be programmed to provide input *or* output delay. Output delay is useful for fixing PCB skew problems.

The performance for Virtex-5 family I/Os is 800 Mb/s single ended and 1.25 Gb/s differential.

LVDS Bandwidth

With its higher-performance differential I/O capabilities and larger packages, Virtex-5 devices are capable of implementing a throughput of 600 x 1.25 Gb/s = 750 Gb/s.

Memory Interfaces

The ChipSync technology built into every I/O enables unmatched reliability for high-performance memory interfaces. It provides adjustable data-to-clock calibration for increased design margins, with a resolution of 75 ps. The adjustment compensates for system variations like process, voltage, and temperature.

Virtex-5 devices can implement wider and faster interfaces for the latest memory architectures. See Table 3.

Table 3: **Bandwidth Performance of Memory Interfaces**

Memory Interface	Data Rate (Mb/s)	Data Width (# of bits)	Bandwidth (Gb/s)
DDR2 SDRAM	667	576	384
QDR II SRAM	600	2 x 324	389
RLDRAM II	600	648	389

Performance-Enhancing Technologies

Virtex-5 FPGAs ensure clock and data signal integrity by incorporating a low-skew, low-jitter 550 MHz differential clock structure. New clock management tiles offer greatly expanded flexibility by combining digital clock managers (DCMs) for precise clock synthesis and phase-locked loops (PLL) for reducing jitter.

Sparse chevron packaging technology and flip-chip assembly techniques, enabled by the proprietary ASMBL technology and abundant PWR/GND pins, improve signal integrity by minimizing package and PCB inductance. On-chip active signal termination technology provides digitally-controlled impedance (DCI) to optimally tune component interconnects while minimizing system component count and cost. For more information, see White Paper WP247, *Virtex-5 Family Advanced Packaging*, at:

http://www.xilinx.com/bvdocs/whitepapers/wp247.pdf.

Lower power consumption per megahertz results in greater performance within your power budget. As Virtex-5 FPGAs reduce dynamic power consumption with 65 nm technology, they also minimize static power consumption with triple oxide

technology. For more information, see White Paper WP246, *Power Consumption in 65 nm FPGAs*, at:

http://www.xilinx.com/bvdocs/whitepapers/wp246.pdf.

Design Entry Methodology and Performance Benchmarks

To further evaluate the performance improvement of the Virtex-5 family, a set of customer designs was implemented with ISE software. The largest improvements were observed on designs with many levels of logic. On these designs, the new ExpressFabric technology improved performance by up to 58% over Virtex-4 FPGAs. Considering all the designs, the performance gain was 30% on average, as shown in Figure 8.

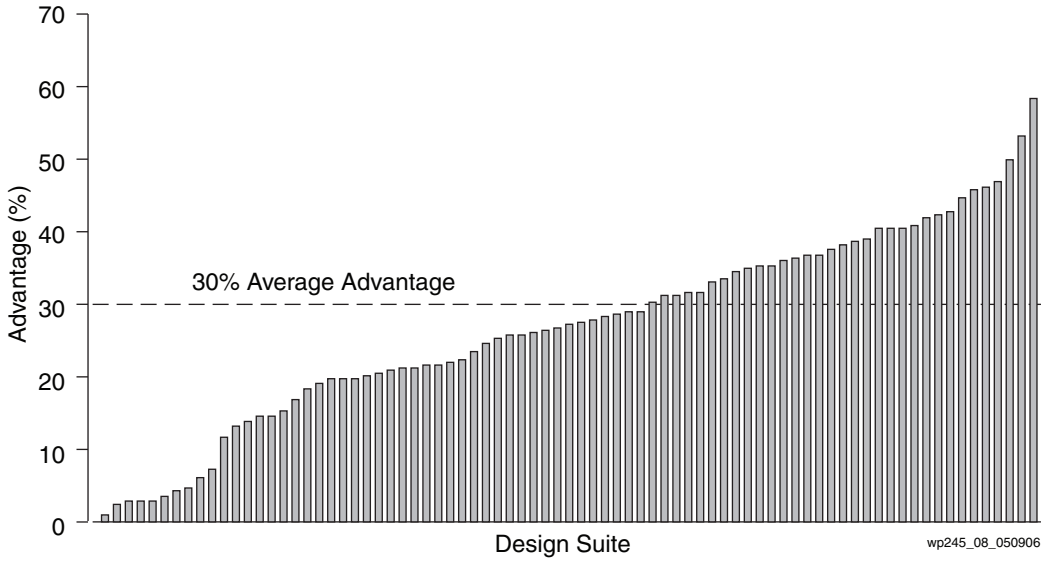

Figure 8: **Logic Performance Benchmarks Comparing Virtex-5 and Virtex-4 FPGAs**

All the designs used in this comparison were RTL-based (VHDL and Verilog). Several of them included CORE Generator™ software EDIF netlists to implement FIFOs and memories.

During synthesis, XST was used, and then ISE place-and-route was run with its effort level set to HIGH. The clock constraints were tightened iteratively by small increments of 5% until negative slack.

For more information and tips on how to achieve the best performance, see the last section of White Paper WP218, *Achieving Breakthrough Performance in Virtex-4 FPGAs* at http://www.xilinx.com/bvdocs/whitepapers/wp218.pdf.

Conclusion

The Virtex-5 family with its new ExpressFabric technology, tightly coupled to other higher-performance hard-IP blocks and I/Os, represents a significant performance boost compared to previous generation architectures.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/12/06	1.0	Initial Xilinx release.
05/17/06	1.1	Updated "DSP" section. This revision is posted on FPGA and Structured ASIC Journal: www.fpgajournal.com.
07/07/06	1.1.1	Typographical edits.