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Xilinx FPGAs Overcome the Side Effects of Sub-40 nm Technology

By: Austin Lesea and Peter Alfke

As CMOS devices follow the technology road map to ever smaller geometries, several undesirable effects have become apparent. These are:

- Soft Errors
- Wear-out Mechanisms:
  - Hot Carrier Injection (HCI)
  - Time Dependent Dielectric Breakdown (TDDB)
  - Negative Bias Temperature Instability (NBTI)
- Latchup

Each issue is reviewed with respect to its effect on system design using ASSP, ASIC, or FPGA devices, and what Xilinx has done to alleviate the potential problems.

Soft Errors

A soft error effect (SEE) describes bit-flips due to cosmic-ray-induced neutron and proton showers (single event upset, or SEU) at sea level or higher as well as voltage transients induced in the logic due to the same energetic particles (single event transients, or SETs).

SEUs are responsible for computer crashes, data corruption, and systems that just suddenly stop working properly. SETs are less likely to crash a system but can also manifest themselves in ways that are similar to SEUs.

In either case, standard cell ASIC/ASSP designs at 40 nm and below have been characterized with over 5,000 failures per billion hours (FIT) per million gates, and over 5,000 FIT per million bits of memory (see [Ref 1] and [Ref 2]). Most ASICs/ASSPs at 40 nm and below contain 5 to 10 million gates and 10 to 40 million bits of memory. Thus, at the high end of that density, there is statistically one soft failure every 0.46 years (250,000 FIT). For 10,000 such ASIC/ASSP devices, there is one failure every 24 minutes; for 1 million devices, there is one failure about every 30 seconds. Unless the application is of trivial importance, this represents a huge problem.

Such soft failures are also impossible to debug because they are gone after the chip is power-cycled or reset; consequently, instead of being able to detect and fix the problem, the user must accept that the equipment is unreliable.

Xilinx® FPGAs are designed to keep the occurrence of SEEs very low; Virtex®-6 devices measure at less than 100 FIT per million bits of configuration, less than 1 FIT per million D flip-flops, and less than 250 FIT per million bits of block RAM. Virtex-6 devices have been tested at Los Alamos Neutron Science Center (LANSCE) in a neutron beam and showed almost half the upsets of Virtex-5 FPGAs.

Ever since 2002, Xilinx IC designers have been finding ways to make the configuration memory cells more robust. Many of these innovations have been patented, and even more are now being tested and evaluated.

The goal is simple: as the arrays grow larger, reduce the soft failure rate even faster, such that the per-device failure rate decreases with each new generation.

The many times better raw FIT rate of Xilinx FPGAs, theoretically, might just compensate for the much larger number of FPGA transistors needed to implement the equivalent ASIC/ASSP functionality. But only a small percentage of configuration bits is actually used in any specific design, and out of those used, not all are critical. That really tips the solution in favor of Xilinx FPGAs. The industry recognizes this difference between measured system failure rate and measured configuration bit upset rate as a large derating factor (see [Ref 3]).

Steps to Reduce System Failure Rate

With Xilinx FPGA devices, the user can take additional steps to reduce or even eliminate the possibility of any system outage. These steps are:

- Block RAM error check and correction (ECC), which reduces the block RAM soft error rate to almost zero (instantiate ECC primitive in Virtex-5 devices.
- Configuration-frame ECC, which reduces the probability of persistent configuration bit-flip failures to almost zero (see [Ref 4] for Virtex-5 devices).
- Triple mode redundancy (TMR), which is performed automatically by the Xilinx TMR Tool (see [Ref 5]).

The system's software and design algorithms must also take into account the potential for a momentary upset. To take advantage of these advanced reliability features in Xilinx devices, the system can be designed to:

- Detect and correct a bad transaction
- Switch to a redundant element (while the first element repairs itself), or
- Reconfigure and restart

When TMR is combined with scrubbing (continuous rewriting of the configuration), or with running frame error correction and block RAM ECC, the total device failure rate can be at single-digit FITs.

Wear-out Mechanisms

Hot Carrier Injection (HCI, see [Ref 6]), Time Dependent Dielectric Breakdown (TDDB, see [Ref 7]), and Negative Bias Temperature Instability (NBTI, see [Ref 8]) are all considered "wear-out" mechanisms, because they all gradually and unnoticeably get worse with time, until the damage or shift is great enough to cause a device to stop working.

The chip designers can choose to adjust these mechanisms to meet their design goals. For example, a high-performance microprocessor might, by choice, accept a wear-out time of seven years in order to meet its performance requirements.

These effects can be reduced by applying lower voltage and temperature stresses, by using thicker oxide, or by designing the circuits to function within the range of threshold shifts that are expected to occur over 20 years of operation. All this results in slightly reduced performance.

Xilinx technology is designed for a less than 0.1% wear-out expectation per device after more than twenty years at maximum junction temperature.

Latch-up

SCR crowbar, or latch-up, can occur when a device has current forced either into or out of the substrate. This can be caused by signal reflections or ground bounce, or if a device is struck by a cosmic ray. At voltages above 1.2V, the parasitic NPNP junctions can latch up in a very low-resistance persistent state, which usually destroys the device.

The chip designer can prevent SCR crowbar by following well-known conservative design rules. If a latch-up mechanism is discovered, it can only be fixed by an expensive chip re-layout, involving new masks.

Xilinx designs are checked for adherence to all the proper design rules. Then, during process qualification, the devices are tested against electrical latch-up according to the JEDEC Standard 8 (see [Ref 9]). As part of the SEU testing, latch-up is also monitored during irradiation in particle streams. The QPro line of components for the aerospace/defense market goes through additional latch-up testing with heavy ions (see [Ref 3]), simulating the harsh environment of space.

Other ASIC, ASSP, and FPGA vendors' products and their cost-reduction standard-cell derivatives have been shown to be sensitive to latch-up, both at 130 nm, and at 90 nm. The device users must make an informed choice to avoid such a meltdown (see [Ref 10]).

Summary

In this paper, we discussed soft errors, hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI), and latch-up in the 40 nm and smaller device-technology nodes. All of these issues need some kind of mitigation. Chip designers must make choices that directly affect the reliability and lifetime of the ASIC, ASSP, or FPGA devices.

Some of these side effects can only be discovered by extensive and usually very expensive testing (high temperature operating life tests, particle beam tests, etc.). And once found, these effects can only be fixed by a complete re-layout of the mask set.

In most cases, unfortunately, such effects are discovered much later by the end user, which leads to costly replacement, potential litigation, and financial losses.

By selecting Xilinx FPGA devices, the user is assured that the necessary design choices have been made correctly, and the testing needed to validate those design decisions has also been performed.

Modern CMOS processes with their smaller geometries cause certain undesirable side effects. Xilinx designers have been aware of these potential problems and have mitigated them in several innovative ways.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/28/07	1.0	Initial Xilinx release.
03/05/07	1.0.1	Tech Pub updates.
08/06/08	1.1	Updated "Soft Errors," "Steps to Reduce System Failure Rate," "Wear-out Mechanisms," and "References" sections.
10/11/11	1.2	Updated for sub-40 nm technology throughout document. Updated "Soft Errors" and "References"sections. Removed Excessive Leakage section.

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