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Timing Closure Exploration Tools with SmartXplorer and PlanAhead Tools

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With the rapid growth of the size and complexity of modern FPGAs, it is increasingly difficult to meet the timing requirements of the design (this challenge is often referred to as a "timing closure" problem). In addition, today's advanced designs are often created by several designers located in different parts of the world, where each designer is responsible for one piece of the design. This complicates timing closure even more.

This white paper describes how SmartXplorer and PlanAhead™ tools can help to achieve timing closure in the shortest amount of time by applying different design strategies and running them in parallel on different machines across a network.

Introduction

To achieve timing closure in the shortest amount of time is a significant challenge when the complexity of FPGA devices doubles approximately every 2 years with designers trying to pack more functionality into a single chip.

Xilinx invests a great deal of time and effort in helping designers overcome such timing challenges by:

- Improving synthesis and implementation algorithms
- Providing graphical analysis tools, such as the PlanAhead tool
- Offering automatic design exploration tools such as SmartXplorer

Although FPGA tools have become easier to use while offering more advanced features, it is difficult to anticipate all design situations. Some timing issues can stay hidden until the final stages of a design cycle, appearing just before product shipment.

Because it is easier, designers, regardless of their experience level, frequently try different tool options before exploring other solutions, e.g., adding placement constraints or changing HDL code. Identifying the best set of strategies for timing closure can be a challenging task, and the user might need assistance to create a solution.

This white paper describes how SmartXplorer and PlanAhead tools help to solve timing problems, the different design cycle stages in which they can be used, and the level of FPGA design experience needed to utilize these tools.

Key Benefits

SmartXplorer and PlanAhead tools have two key features:

- They automatically perform design exploration by using a set of built-in or user-created implementation strategies to try to meet timing.
- They allow running these strategies in parallel on multiples machines, completing the job much faster.

Design Strategies

A design strategy is a set of tool options that are intended to achieve a particular design goal such as reduced area, faster speed, or reduced power. A designer, based on requirements, experience, and design expertise, can decide how to deploy the design strategies. For both experienced and novice FPGA designers, SmartXplorer and PlanAhead tools facilitate the search for the best solution through the multitude of available timing optimization choices.

SmartXplorer and PlanAhead tools increase the probability of meeting timing. For example, if forced to make design modifications that cause some timing constraints to fail, an experienced designer can analyze and debug the design using graphical tools, such as FPGA Editor or PlanAhead software. While debugging the design, the experienced designer can also launch SmartXplorer or PlanAhead tools to run all predefined strategies in parallel to try to meet timing. In this case, both tools increase the designer's ability to overcome the timing problems at minimum cost (i.e., no design modification and no need for new functional simulations).

Even in the hands of an experienced designer, a design can still be picoseconds away from meeting its timing requirements. SmartXplorer and PlanAhead tools can be used to identify the final few picoseconds of slack needed.

SmartXplorer and PlanAhead tools can also be used by a novice designer who has limited experience with FPGA design flow. For example, if a novice designer is trying to complete a project and the post place and route timing fails, the next steps taken might include modifying the HDL, using placement constraints, or changing design strategies. However, SmartXplorer and PlanAhead tools can evaluate different strategies and then determine the best design option.

SmartXplorer and PlanAhead tools are delivered with a built-in set of predefined strategies. Tested, predefined strategies are provided with the most effective techniques for achieving better performance. The predefined strategies also eliminate the need for the designer to learn new options with each new version of ISE® software.

The predefined strategies delivered with SmartXplorer are tuned and selected separately for each FPGA family. This selection is revised for each major release to ensure the best possible correlation with the latest software version. The PlanAhead tool also provides the most commonly used strategies to meet timing closure.

Many customers create their own design strategies or scripts based on their experience. SmartXplorer and PlanAhead tools allow users to integrate their custom strategies into the system and either exclusively use them or combine them with the predefined strategies.

The PlanAhead tool offers a powerful and flexible graphical interface to create and manage design strategies. See Figure 1.

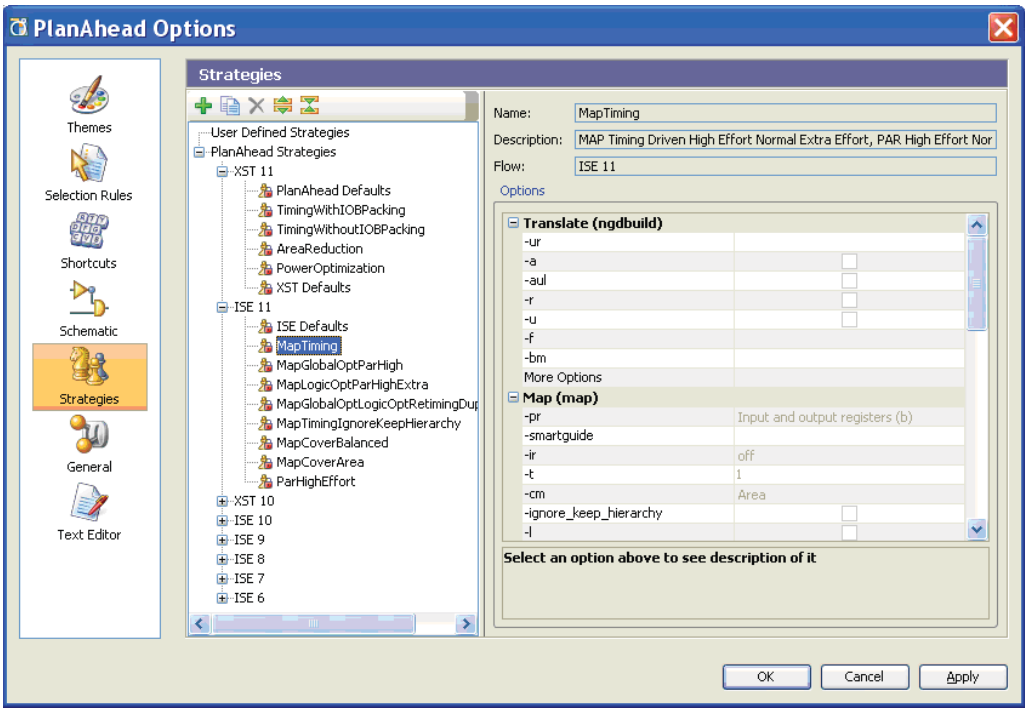

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Figure 1: **PlanAhead Tool Strategies**

SmartXplorer and PlanAhead tools are not simply for use during the late, time-limited portion of the design cycle. They can be used during the entire project cycle, preventing or reducing the magnitude of timing issues. These tools should be run on a regular basis to monitor the design and ensure that the timing results stay within an acceptable range.

Parallelism

The ability to execute several design strategies (jobs) in parallel is a powerful feature that allows designers to complete the project faster. This capability is operating-system dependent.

Linux OS

SmartXplorer and PlanAhead tools can run multiple jobs in parallel on different machines across the network. This can be done in two ways:

- Typical Linux network: Both tools manage the job distribution across the network. The designer has to provide a list of machines that can be used.
- Load Sharing Facility (LSF) or Sun Grid Engine (SGE) compute farms on the network with SmartXplorer: LSF or SGE manages the job distribution. The designer has to specify the number of machines that can be simultaneously allocated to SmartXplorer.

If the designer does not have access to the Linux network but has a personal Linux machine with a multicore processor or several processors, several jobs can still be run in parallel on this single machine.

Microsoft Windows OS

SmartXplorer and PlanAhead tools allow several strategies to be run in parallel on a single Windows machine if it has a multicore processor or several processors.

Using a Single Linux or Windows Machine

If access to a Linux server on a network is unavailable and only a local computer can be used, the computer must have at least one multicore processor or several processors.

The designer then needs to estimate how many jobs the computer can run simultaneously. Theoretically, the number of jobs that can be run in parallel can be calculated as:

$$\text{Nb\_Of\_Jobs} = P * C$$

Where P is the number of processors, and C is the number of cores per processor.

For example, if the computer has four dual-core processors, the designer can run eight jobs in parallel.

However, depending on the available memory, its speed, the speed of its hard drive, the computer might not be able to efficiently operate with the maximum number of jobs calculated using the above formula. In this case, the designer might choose to reduce the number of jobs to be executed simultaneously.

Here are tips for the designer:

- If due to the memory requirements, the computer can only run a single strategy at a time, the designer has to run all strategies sequentially.
- When trying to solve timing problems, the designer should consider isolating the timing critical blocks and using the tools to optimize these critical portions of the design. This enables the computer to manage multiple strategies in parallel for these smaller blocks. If this is the case, parallel jobs should be enabled to save time.

Design Environment

The PlanAhead tool is targeted for users who are seeking to run multiple implementation strategies for their designs along with the PlanAhead tool's powerful design analysis, floorplanning, and pin assignment capabilities. SmartXplorer is for ISE software users, running Xilinx® tools either from command line or Project Navigator environment.

The overall job execution progress can be monitored by using the Design Runs View in the PlanAhead tool and Status Table in SmartXplorer. They are dynamically updated and contain the list of strategies and corresponding timing results.

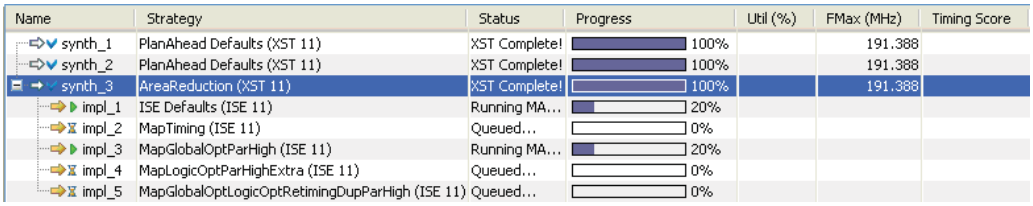

Figure 2: **PlanAhead Tool Design Runs View**

Strategy	Host	Status	Timing Score	Run time
ParHighEffort2	None	None	None	None
ParHighEffort1	None	None	None	None
MapUseIOReg	None	None	None	None
MapTimingExtraEffort	tripoli	Done	4413	00h 00m 49s
MapTiming2	None	None	None	None
MapTiming1	None	None	None	None
MapPhysSynthesis	tripoli	Mapping	None	00h 00m 04s

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Figure 3: **Status Table in SmartXplorer**

The command line users can monitor the progress by opening an HTML file in a web browser.

Strategy	Host	Output	Status	Timing Score	Total Run Time
MapTimingExtraEffort	xgr-sweng135	run1	**Done**	4413	0h 0m 39s
MapPhysSynthesis	xgr-sweng135	run2	Mapping	None	0h 0m 4s
ParHighEffort1	None	None	None	None	None
ParHighEffort2	None	None	None	None	None
MapTiming1	None	None	None	None	None
MapTiming2	None	None	None	None	None
MapUseIOReg	None	None	None	None	None

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Figure 4: **SmartXplorer HTML Run Progress**

Using the PlanAhead tool, all report files generated by design strategies can be accessed directly from the Monitor or Reports tab in the Implementation Runs Properties view.

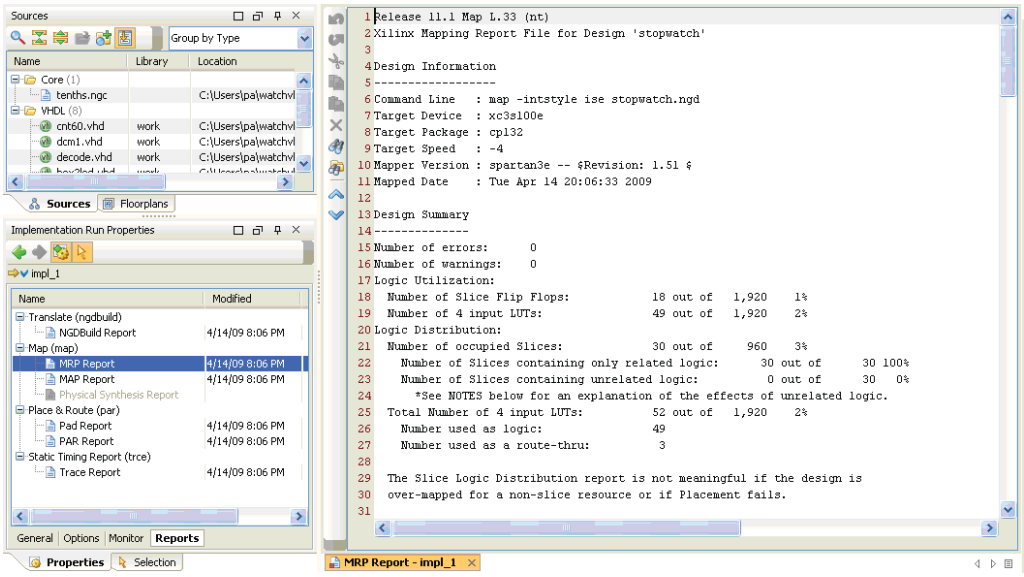

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Figure 5: **PlanAhead Tool Implementation Run Reports**

In Project Navigator, all report files can be accessed via Design Summary generated for each strategy.

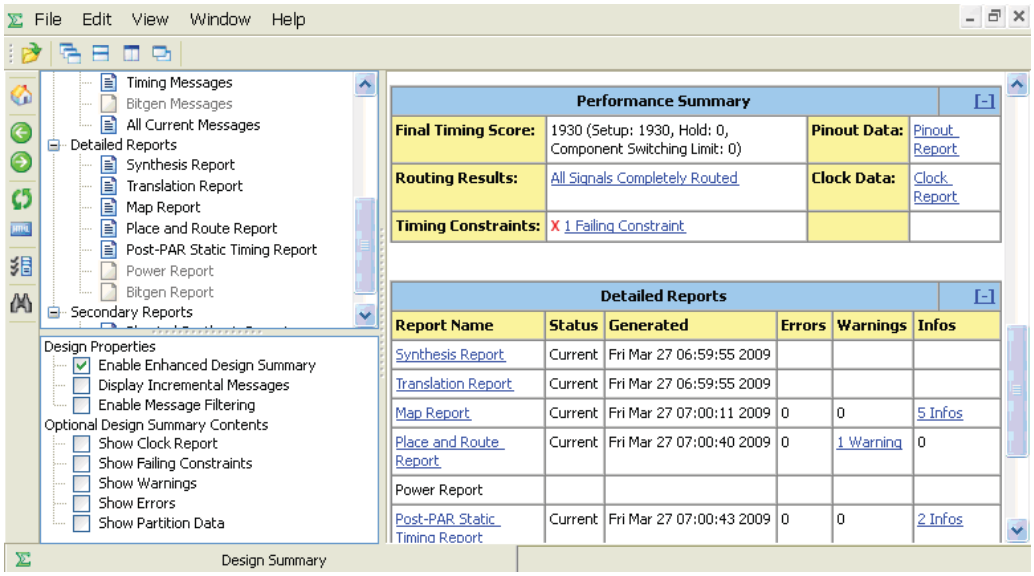

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Figure 6: **Project Navigator Reports**

Conclusion

The SmartXplorer and PlanAhead tools help users to achieve timing closure by using a set of predefined built-in strategies. In addition, both tools allow users to create and integrate their own design strategies into the system and either exclusively use them or combine them with the predefined strategies.

The ability to execute several design strategies in parallel is a powerful feature of the SmartXplorer and PlanAhead tools, which allows designers to complete the project in the shortest amount of time.

The SmartXplorer and PlanAhead tools are not simply tools to use during the late, time-limited portion of the design cycle. They can be used during the entire project cycle, preventing or reducing the magnitude of timing issues.

Additional Resources

For the latest information on SmartXplorer and PlanAhead tools, including video demonstrations, tutorials, white papers, and user guides, see:

http://www.xilinx.com/tools/logic.htm

http://www.xilinx.com/tools/planahead.htm

The screen captures in this document are conceptual representations of their subjects and provide general information only.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
08/26/09	1.0	Initial Xilinx release.

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