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IBIS Model Usage

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Models of I/O characteristics are used to accurately simulate the signal behavior on a printed circuit board. Most designers are familiar with SPICE models, but a given manufacturer's SPICE models contain information that is considered to be proprietary. Therefore, simpler models are devised that extract the SPICE parameters and present them to the user in such a way that the proprietary information is protected. One such form is the I/O buffer information specification (IBIS) format. This white paper describes some of the features of the IBIS format as well as how to use them.

What Is an IBIS Model?

IBIS models represent the I/V characteristics and dV/dt for the best case, typical case, and worst case inputs and outputs. Simulations of complete I/O chains can describe printed circuit board transmission line effects. Ringing, bounce, and crosstalk can be predicted, corrected, and controlled using IBIS.

Can IBIS Predict Ground Bounce?

IBIS models contain package parasitic information for simulation of ground bounce. Although the data is available within the model file, not all simulators can use it to simulate ground bounce. There is a possibility that the simulation results will not agree with the actual results due to package, die, and printed circuit board ground plane modeling problems. For the same reason, simultaneous switched outputs (SSOs) are also difficult to model and only a first approximation is provided to the designer even if the tool provides the feature.

Can IBIS Provide Timing Information?

IBIS, version 2.1 does not provide chip-internal delay. IBIS is used to simulate transmission lines and analyze signal integrity issues. IBIS simulations can be used to show the difference in timing by modeling the termination used in the data sheet specifications, and then modeling the termination used in the actual application. The resulting time difference is used to correct the data sheet specification for the application.

What Tools Can Be Used with IBIS?

SPICE circuit emulation tools that import IBIS models and make use of them are available. However, other available tools can be easier to use and are less prone to errors that result from operator skill and training issues. One such tool is the HyperLynx tool by Mentor Graphics, which can be downloaded from http://www.mentor.com/hyperlynx. IBIS tools are available for most popular design programs.

Where Can the IBIS Models Be Found?

IBIS models are available at http://www.xilinx.com/support/download/index.htm. On the ensuing page, select **IBIS Models** from the Select a Download Type pull-down menu, and then select the device family from the respective pull-down menus.

Tips on Using IBIS Models and Tools

- Obtain the latest IBIS model from the Xilinx website.
- Choose the correct Xilinx I/O model for the output you are using: LVTTL, GTL, LVCMOS, and so on. *This is critically important.* Separate IBIS files can exist because the I/Os are programmable. Only the correct IBIS file will yield the correct results. Consider this example of a Virtex™ FPGA: OBUF_F_2 defaults to

an LVTTL, FAST slew rate, 2 mA drive strength output buffer. The IBIS file that matches the programmed output must also be specified in the simulator.

- IBIS models the process corners by using minimum, typical, and maximum data. The terms “fast-strong,” “typical,” and “slow-weak” are used by some of the IBIS modeling tools to describe these same process corners. For each I/O type, these three corners defined by the IBIS standard represent the maximum variability for the device due to the manufacture of the device. Do not confuse “fast-strong” with the Xilinx FAST option—they are not the same. “Fast-strong” describes what the fastest and strongest I/O can look like. FAST is a selection for a non-slew rate limited output, which customers are able to control.
- Model “weak-slow,” “typical,” and “strong-fast” to ensure that ringing, bounce, and crosstalk are under control in all cases. If the modeling tool has electromagnetic interference (EMI)/radio frequency interference (RFI) prediction, choose the strongest process corner for that analysis (fastest edges = highest RFI).
- Ensure that the printed circuit board stackup is specified on the fabrication control drawing so that the physical dimensions remain constant. If the material used by the printed circuit board vendor is not specified, whatever is in stock will be used. The thickness of the layers will thus vary, resulting in the impedance varying from what was assumed by the modeling tool.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/27/08	1.0	Initial Xilinx release. Based on a previously published *Tech Xclusive* article by the same author.

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