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New High Speed Broadcast Video Connectivity Solution (3G) with Low-cost FPGAs

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Using Xilinx Spartan™-3E and Spartan-3A FPGAs, a National Semiconductor PHY, and a Xilinx video processing stack provides a very cost-effective and flexible approach to the challenges of multi-rate broadcast.

Introduction

Today's designers of high speed video applications have a significant challenge to address both the digital IP and analog physical interface requirements of their products. Trying to support both in one ASSP chip often compromises the quality or cost-effectiveness of the solution, since digital and analog components often have very different requirements. It can also be difficult to find a solution that has exactly the right IP and the right physical interface without waste in either area, or with the ability to change to meet the requirements of multiple standards.

The new chip set featured by Xilinx and National Semiconductor combines the best of the digital and analog worlds into one highly integrated solution. The digital solution, including the video processing IP stack, is handled by the proven Spartan-3E or Spartan-3A FPGA silicon. The analog section is handled by the proven National Semiconductor SDI PHY products for the greatest signal quality with the lowest jitter. It allows professional audio/video broadcast system developers to concentrate more on their own specific video content processing functionality and IP instead of the front-end interface connectivity.

SDI Video Standards

Serial digital interface, or SDI (*SMPTE 259M*), is a broadcast industry standard widely adopted to transport uncompressed standard definition (SD) video signals over a single coaxial cable. By definition, SDI typically supports data rates of 270 Mbps to cover screen formats of 480i at 60 Hz (480i60).

High Definition SDI, or HD-SDI (*SMPTE 292M*), boosts the bit rate up to 1.485 Gbps to support high definition formats like 720p60 and 1080i60.

The standard 3 Gigabit SDI, or 3G-SDI (*SMPTE 424M*), further extends the serial digital throughput up to 2.97 Gbps in order to carry the highest screen resolution 1080p60.

National Semiconductor PHYs

National Semiconductor offers a complete portfolio of products supporting the physical layer transmission for SDI applications. National's new family of SDI serializers and deserializers have speed grade options supporting standard definition (SD) *SMPTE 259M* at 270 Mbps, high definition (HD) *SMPTE 292M* at 1.485 Gbps, and the 3 Gbps standard (3G-SDI) *SMPTE 424M* at 2.97 Gbps. Table 1 details the PHY product information.

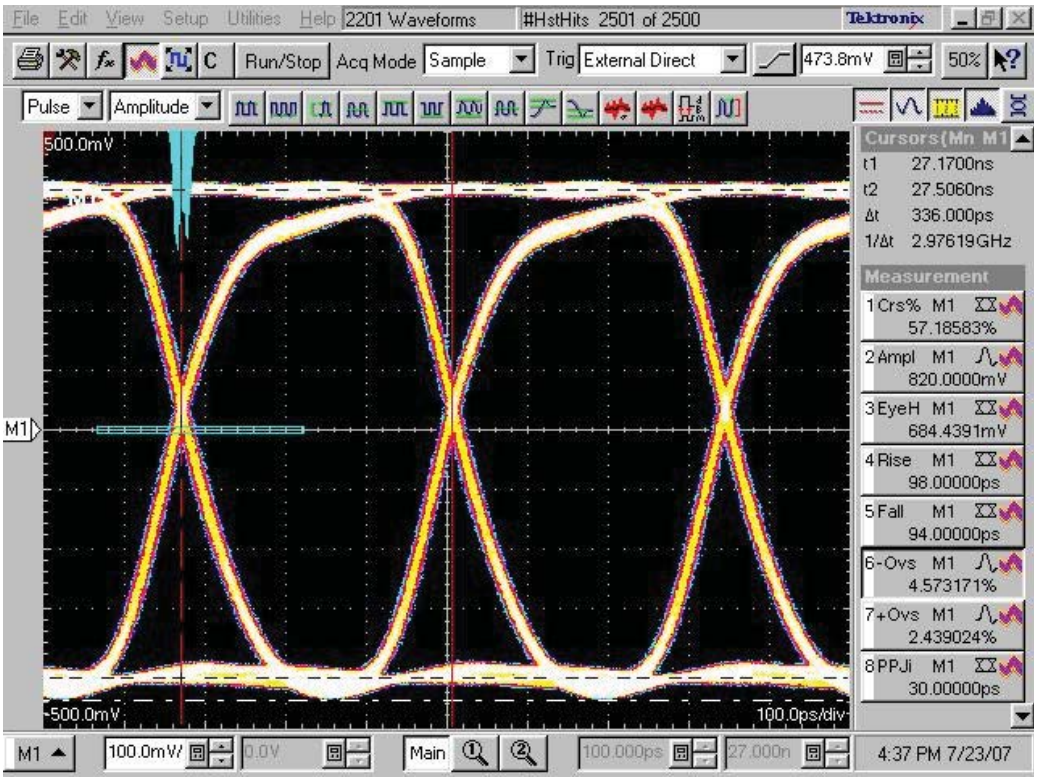
Table 1: **National Semiconductor PHY Families**

Product ID	Description	Max Data Rate	Data Rates Supported	SMPTE Standards Supported
LMH0340	Serializer and Driver	3G	2.97G 1.485G 270M	424M 292M 259M
LMH0341	Reclocking Deserializer	3G	2.97G 1.485G 270M	424M 292M 259M
LMH0040	Serializer and Driver	HD	1.485G 270M	292M 259M
LMH0041	Reclocking Deserializer	HD	1.485G 270M	292M 259M
LMH0050	Serializer	HD	1.485G 270M	292M 259M
LMH0051	Deserializer	HD	1.485G 270M	292M 259M
LMH0070	Serializer and Driver	SD	270M	259M
LMH0071	Reclocking Deserializer	SD	270M	259M

National Semiconductor's LMH034x family highlights superior analog performance:

- Ultra-low Output Jitter: 50 ps typical at HD and 3 Gbps rates (see Figure 1)
- Exceptional Input Jitter Tolerance: 0.6UI minimum (see Figure 2)
- Integrated high precision PLL for serial clock reference and data recovery
- Integrated cable driver in LMH0340 transmitter
- Integrated Serial Re-clocked Loop Through and driver
- Low Power Consumption
  - Tx: 435 mW
  - Rx: 590 mW
- No external VCOs or clock required

Figure 1 and Figure 2 show the low output jitter and input jitter tolerance.



Equipment: Tektronix CSA8000 sampling scope with 20 GHz sampling heads
Input Signal: PRBS 2^{15} -1
Data Rate: 2.97 Gbps

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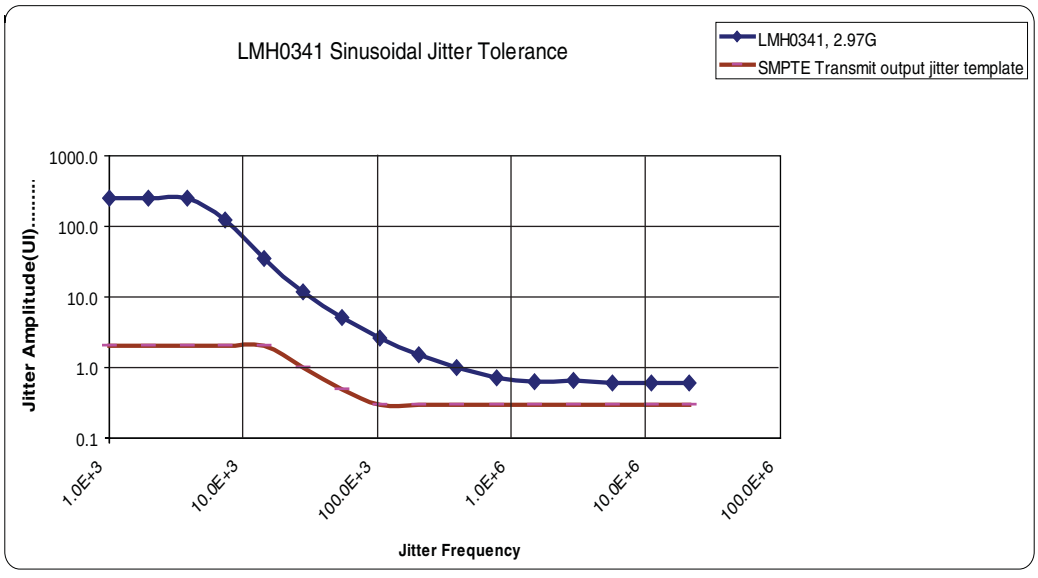
Figure 1: **LMH0340 3 Gbps Output Jitter: 30 ps at HD and 3G Rates**



Data Rate: 2.97 Gbps
Equipment: Agilent J-BERT

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Figure 2: **LMH0341 Minimum Input Jitter Tolerance: 0.6UI**

In addition to leading-edge analog performance, National's LMH family reduces the traditional parallel bus between the PHY device and the host FPGA from a 20-bit single-ended interface to a 5-channel Low-Voltage Differential Signaling (LVDS) interface. This innovative narrow differential bus reduces EMI and simplifies board layout by reducing the number of traces on the interface and using fewer pins on the host FPGA. Additionally, National's discrete PHYs do not require any external VCOs or jitter reducing PLLs. Figure 3 and Figure 4 show the simplified results of using an LVDS interface.

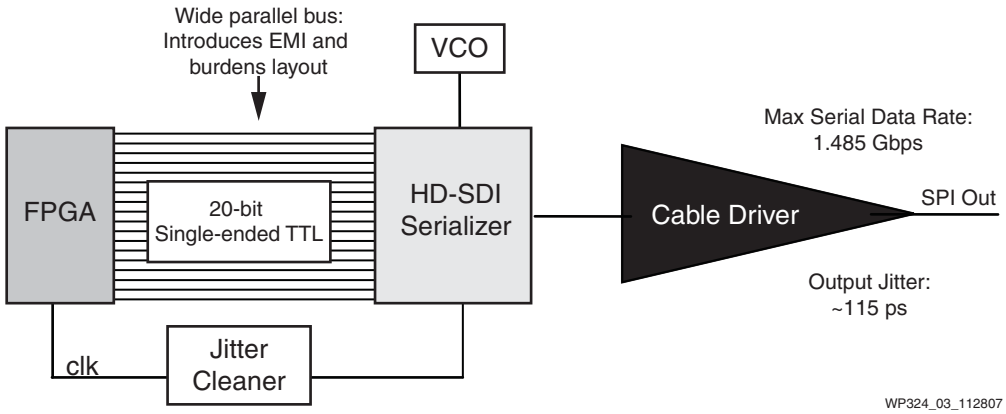

Figure 3: **Then: SDI Bill of Materials with a Wide Parallel Bus**

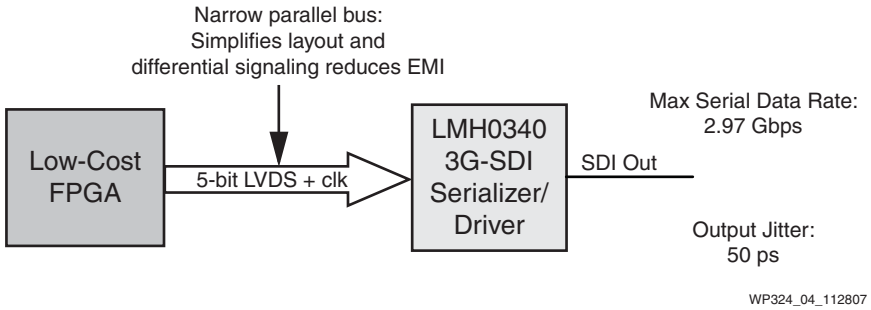

Figure 4: **Now: SDI Bill of Materials Reduction with a Narrow Parallel Bus**

The combined National/Xilinx Spartan solution brings low-cost FPGAs into the high-end broadcast market supporting SD, HD and 3 Gbps data rates for professional video applications.

Spartan-3E and Spartan-3A FPGA Features for Video Applications

The Spartan-3E and Spartan-3A FPGA families suit many aspects of video applications by offering high performance, high density (logic and I/O), great flexibility and scalability with unique, cost-effective features, such as:

- 50,000 to 1.6 million system gates
- True LVDS differential I/O drivers at over 666 Mbps with internal termination on receiver for direct chip-to-chip communication
- Double Data Rate (DDR) I/O registers at over 300 MHz to increase effective bandwidth beyond 600 Mbps
- 18Kb Dual Port Block RAMs at over 200 MHz for FIFOs and data buffering

- Dedicated 18x18 Multipliers at over 200 MHz for high-speed digital signal processing
- Digital Clock Managers (DCMs)
  - Clock deskew
  - Frequency synthesis
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 300 MHz)
- Full programmability to easily modify the design during development or in the field, or to support multiple standards in a single solution
- Software and IP to quickly implement key features of video applications
- Design examples and reference boards to get started quickly

By using FPGAs, you can be compliant to industry standards while differentiating yourself from your competitors. Such differentiation may be too difficult to find using an ASSP solution, and too expensive to address with an ASIC. The flexibility of a programmable solution provides faster time-to-market, and field updates provide longer time-in-market. Numerous standards (and versions) cause uncertainty so designs need flexibility in transmission schemes, MPEG profiles, display formats, color correction, etc.

Further detailed descriptions about the Spartan-3 Generation FPGA features can be found at:

www.xilinx.com/products/silicon_solutions/fpgas/spartan_series/index.htm

Interconnect Soft SerDes and Video Processing IP Stack

While the National Semiconductor PHY takes care of the SDI physical interface, the FPGA plays an essential role in supporting all digital functions in the video processing IP stack, including:

- 20:5/5:20 LVDS Soft Serialization and De-serialization (SerDes)
- SMPTE Scrambling/Descrambling
- Video Framer/De-framer
- CRC and Line Number Insertion
- Rasterization
- ANC Insertion
- Video Standard Detection and Flywheel

The FPGA design is divided into the two frequency domains of "soft SerDes" and "pixel processing," as shown in Table 2.

Table 2: **FPGA Design Frequency Domains**

Standard	Soft SerDes	Pixel Processing
SD-SDI	27 MHz	27 MHz
HD-SDI	148.5 MHz	74.25 MHz
3G-SDI	297 MHz	148.5 MHz

The clock frequency used in the "soft SerDes" is typically only half of the serialization bit rate. This is accomplished by leveraging the DDR technique. The pixel processing clock frequency on the other hand is determined by the relevant video transmission format, for instance 74.25 MHz for 720p60 and 148.5 MHz for 1080p60.

The timing closure challenge is mainly on the "soft SerDes" side because up to 297 MHz operation is required to achieve 594 Mbps across all the differential channels. The Xilinx Spartan Applications team has been offering this soft SerDes reference design in a beta version since May 2007. Since then, extensive testing has been done between Xilinx and National Semiconductor. All three data rates have passed BERT test suites developed by Xilinx. Figure 5 and Figure 6 illustrate the basic SerDes construct.

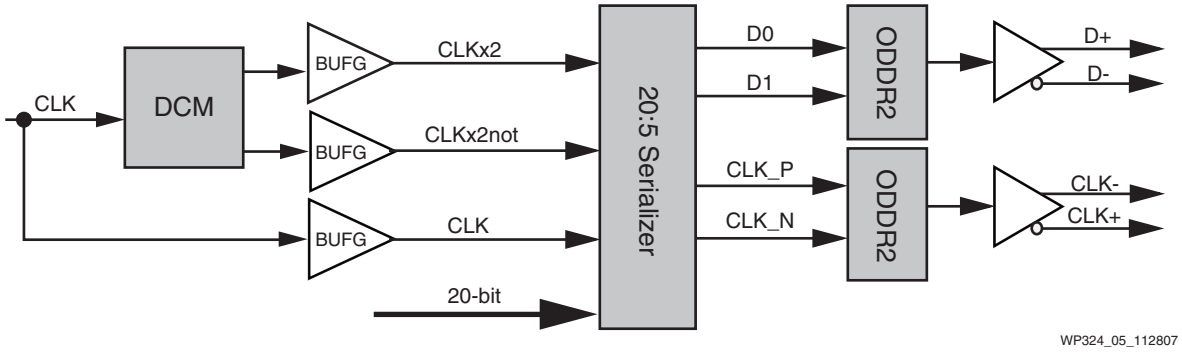

Figure 5: **Basic Soft SerDes Construct in Spartan-3E FPGAs: 20:5 Transmitter**

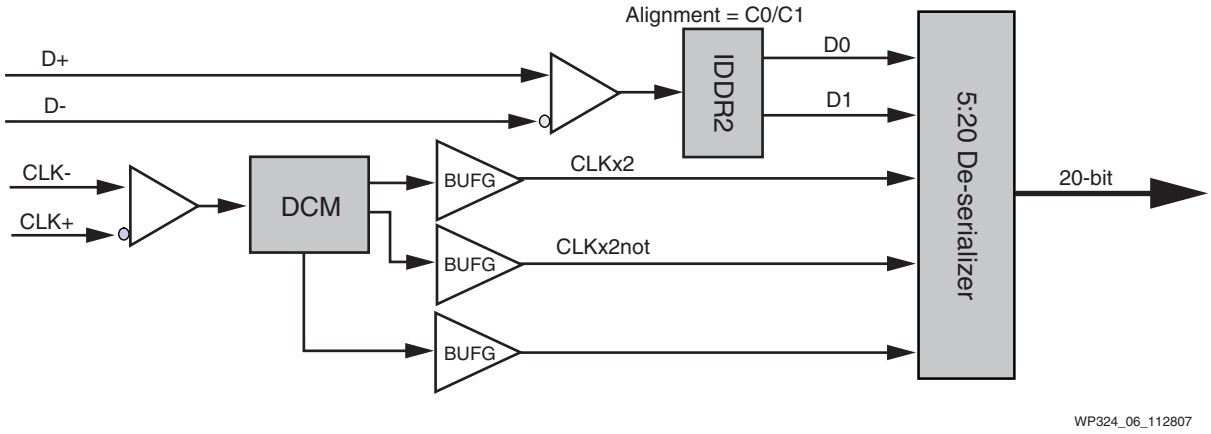

Figure 6: **Basic Soft SerDes Construct in Spartan-3E FPGAs: 5:20 Receiver**

Xilinx has a long history of supporting SDI interfaces in the Virtex™ family of FPGAs. XAPP514, *Audio/Video Connectivity Solutions for the Broadcast Industry*, the reference design book developed by Xilinx Virtex Applications team, details all aspects of the video processing stack including SDI, HD-SDI, DVB-ASI, SDTV/HDTV test pattern generation and even embedded audio. Active work has been done by Xilinx and National Semiconductor to port these highly valuable reference designs into Spartan-

3E and Spartan-3A FPGAs. Figure 7 illustrates a list of successfully ported reference blocks used for demonstration purpose based on an internal evaluation board.

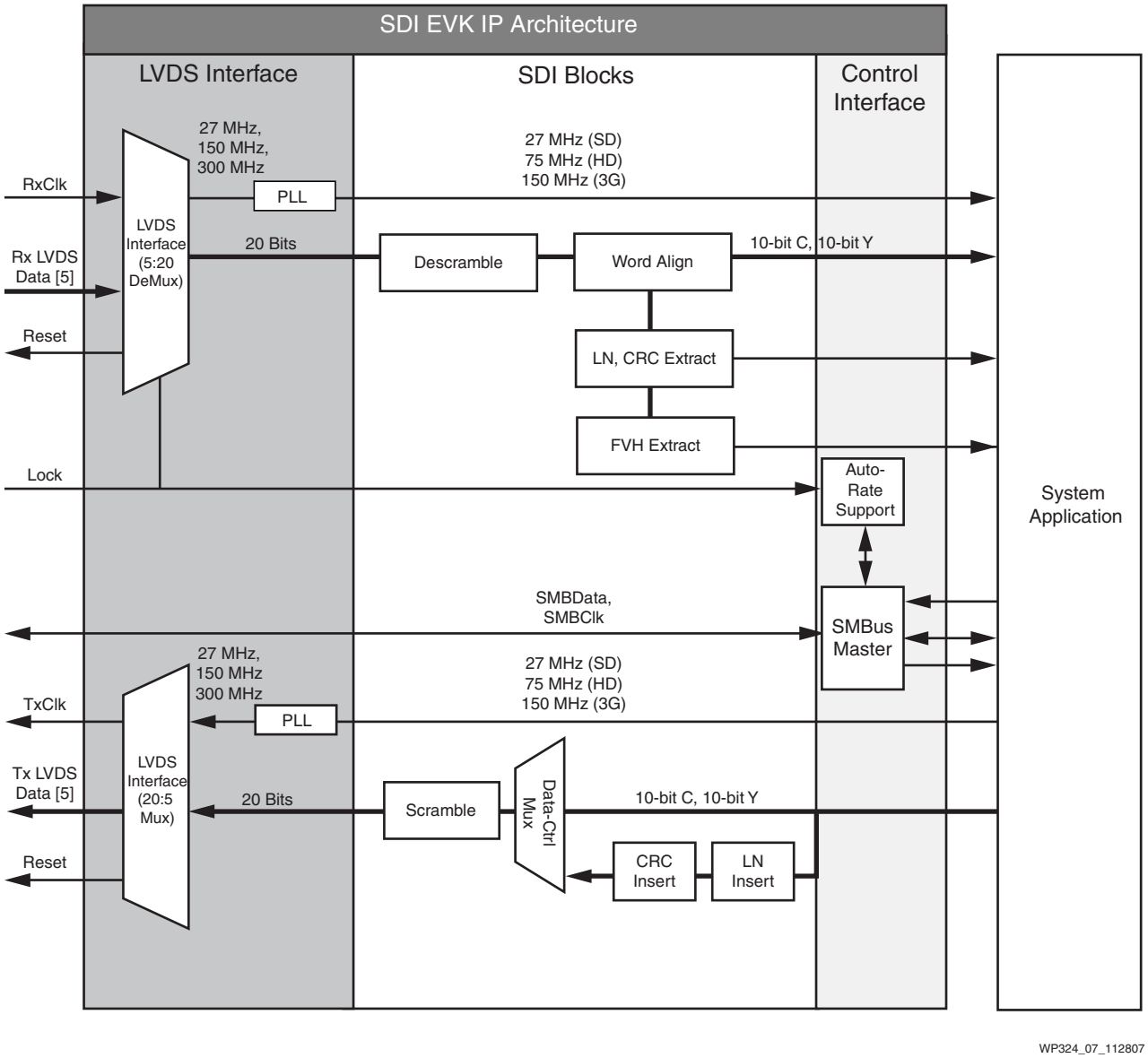

Figure 7: **Successfully Ported Reference Blocks from XAPP514**

Figure 8 illustrates a SMPTE 75% color bar display generated by the board. For more information on this IP, see XAPP514, *Audio/Video Connectivity Solutions for the Broadcast Industry*.

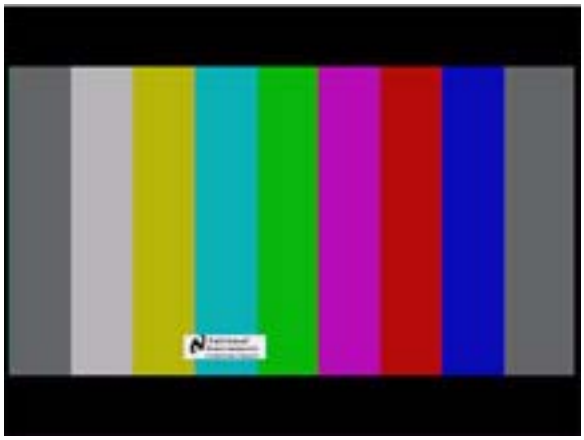

Figure 8: **HDTV Color Bar Generation**

Many of the XAPP514 designs are being retargeted and updated for use in additional Spartan-3 Generation and Virtex-5 FPGAs. New designs will be published for audio embedding and de-embedding in video streams, as well as support for Dual Link HD-SDI, 3G-SDI Levels A & B, and conversion between standards. See www.xilinx.com for the latest documentation.

Target Applications

Xilinx low-cost Spartan-3 Generation FPGAs have been used successfully in a wide range of consumer and professional video applications. These include a JVC professional broadcast HDV camera/recorder using the Spartan-3E FPGA (see the press release on this solution for more information).

The combination of the Spartan FPGA for digital logic and National Semiconductor PHY for the analog interface opens up new possibilities in high-end applications in professional video, broadcasting, and digital cinema. Applicable products include high-definition video cameras, digital video recorders, video editors, and display monitors.

Conclusions

The power of Xilinx Spartan-3E and Spartan-3A FPGAs combined with a proven National Semiconductor SD/HD/3G-SDI transceiver and the XAPP514 video processing IP delivers a truly cost-effective solution to the ever-increasing data

throughput requirements of broadcast video applications. Figure 9 shows an example of an application block diagram using this solution.

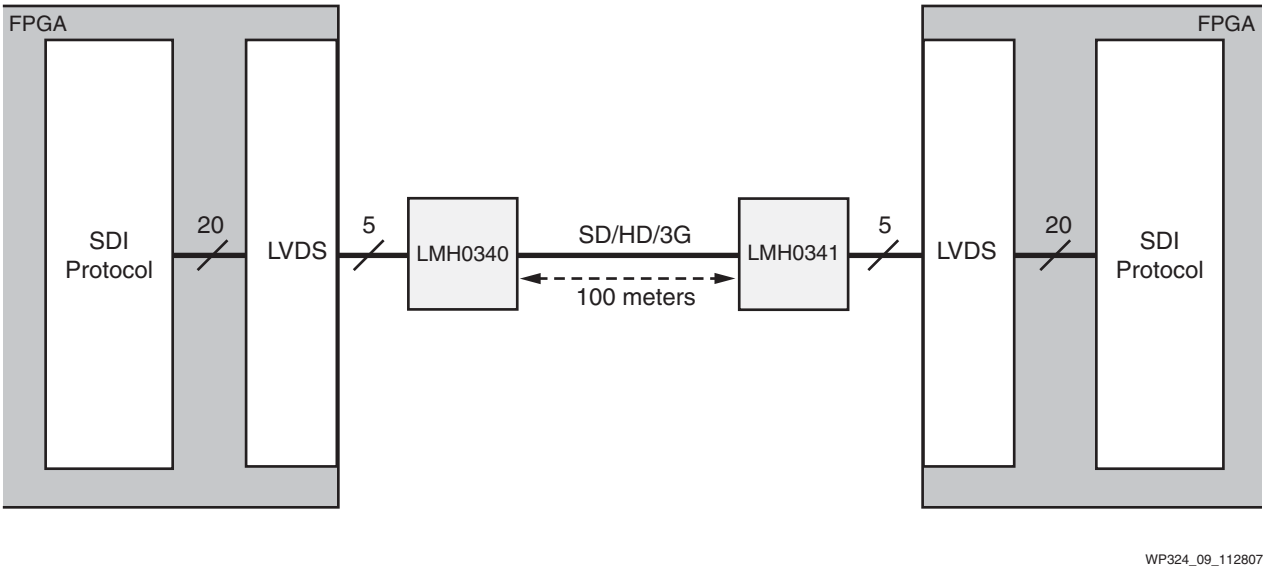

Figure 9: **Typical Application Block Diagram**

While the complete hardware solution is available today, a complete SDI evaluation kit will be offered by the Xilinx distribution partner Avnet in the first quarter of 2008.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/28/07	1.0	Initial Xilinx release.

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