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Xilinx 7 Series FPGAs: The Logical Advantage

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Configurable logic tiles are the fundamental building blocks of all programmable digital electronic systems. Ever since Xilinx invented the FPGA in the 1980s, configurable logic, in the form of look-up tables and registers, has been an essential component of digital electronics systems across all markets and applications.

This white paper describes the features of the configurable logic block in the 28 nm Xilinx 7 series FPGAs, highlighting advantages over previous Xilinx FPGAs and the benefits that these changes bring to the digital design engineer.

The versatile logic structure allows a vast array of logical and memory functions to be implemented in a single resource, providing capability and efficiency in performance, power, and cost.

Introduction

The configurable logic block (CLB) is the core of the logic structure of Xilinx FPGAs. Within a CLB reside slices that consist of look-up tables (LUTs), carry chains, and registers. These slices can be configured to perform logical functions, arithmetic functions, memory functions, and shift register functions. Over the years, the quantity of resources within a CLB has evolved to continuously provide the optimum capability at the right cost. The original Virtex® and Spartan®-II architectures, which were introduced around the turn of the millennium, provided a CLB consisting of two slices, where a slice contained two four-input LUTs and two registers. Since then, a slice has changed significantly—in 7 series FPGAs, a slice consists of four six-input LUTs (LUT6) and eight registers, as shown in Figure 1.

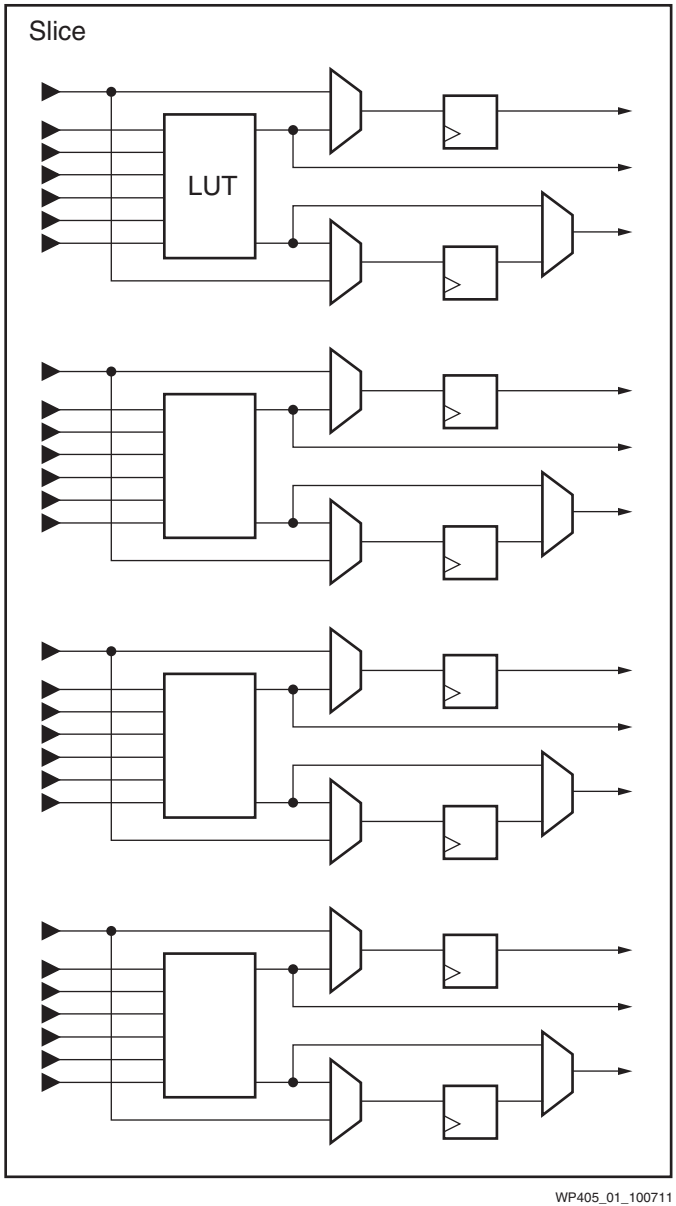

Figure 1: **Slice Architecture in 7 Series FPGAs**

Slice Architecture in 7 Series FPGAs

All 7 series FPGA families (Artix™-7, Kintex™-7, and Virtex-7 devices) use the same logic architecture: CLBs consisting of two slices. Slices in the 7 series FPGA architecture come in two varieties—those that are capable of implementing logical, shift register, and memory functions in the LUT, called SLICEM, and those that can only implement logical functions in the LUT, called SLICEL. Employing this strategy of full feature SLICEM combined with reduced feature SLICEL enables the optimum capability and performance while maintaining low cost and low power. The 7 series FPGA slice architecture is based closely on the slice architecture introduced in the Virtex-6 and Spartan-6 families. The similarity between the Virtex-6, Spartan-6, and 7 series FPGA slice architecture provides an easy migration path for existing designs and IP into 7 series FPGAs; designers can migrate their designs to the latest features and highest performance, lowest power devices with minimal redesign effort. Additionally, using the same scalable, optimized architecture for all 7 series FPGAs allows designs originally targeting one 7 series FPGA family to be ported easily to another 7 series FPGA family.

Slices are combined in a CLB in pairs with either two SLICEL or one SLICEL with one SLICEM. The 7 series FPGAs are built on the column-based ASMBL™ architecture, which allows for the easy placement of resources where the designer needs them. In this case, the memory-capable slices are most prevalent in proximity to the columns of DSP slices, providing designers storage for coefficients close to where they are required. Xilinx design tools have full knowledge of the relative placement of resources and intelligently and automatically map a design to the resources in the most efficient way while adhering to any constraints specified by the user.

Figure 2 shows how the LUT and registers are arranged in relation to one another. Figure 2 only includes one LUT and its associated two registers and omits the carry chain. In a full slice, there are four LUTs and eight registers.

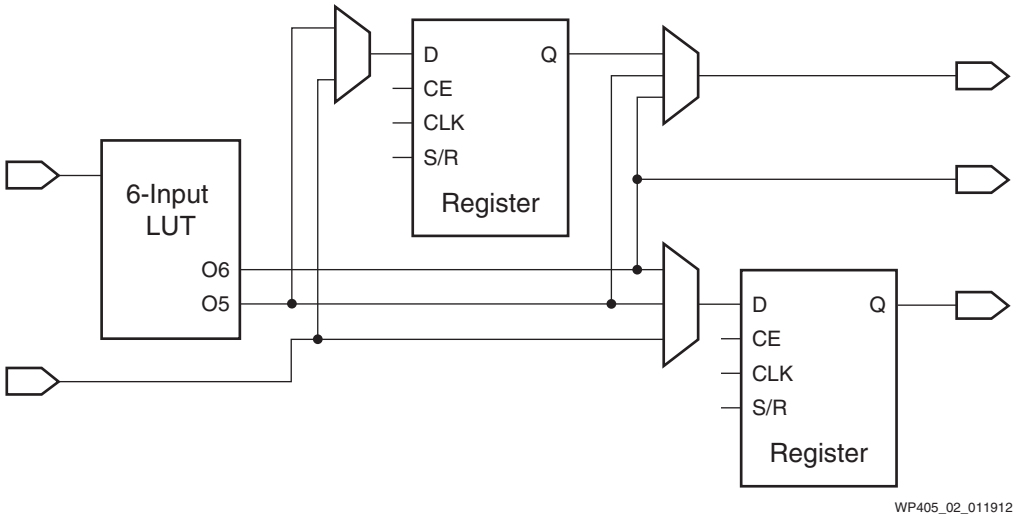

Figure 2: **Layout of 6-Input LUT and Two Registers within a Slice**

The 6-input LUTs are capable of implementing any Boolean logical function that is a product of six input signals but can also be split into two five-input LUTs—as long as the two functions share common inputs. Additionally, a LUT in a SLICEM can be configured as 64 bits of Distributed RAM or up to 32-bit Shift Register Logic (SRL) functions. For more information, see UG474, *7 Series FPGAs Configurable Logic Block User Guide*.

Common Slice Resource Usage

Versatility is fundamental to programmable logic; designers can use the FPGA slice resources in numerous ways depending on their objectives.

The architecture allows the LUTs to be used independently from the registers. The Bypass (AX/BX/CX/DX) input to the slice allows access to the D input of the registers without going through the LUT, and the combinatorial signals are fed to the output of the slice (Figure 3).

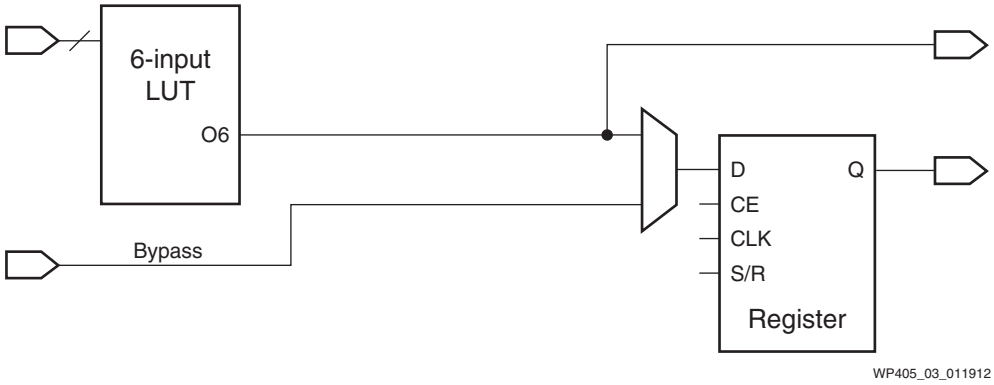

Figure 3: **Use of Bypass Input to Access the Slice Register**

In addition to driving the register directly, the Bypass input can be used to drive the carry chain.

The LUT outputs can feed directly into the D input of the associated registers using the flip-flop multiplexers (Figure 4). The O5 LUT output can be connected to the input of either register (Figure 4), whereas the O6 LUT output can only connect to one of the registers (Figure 2).

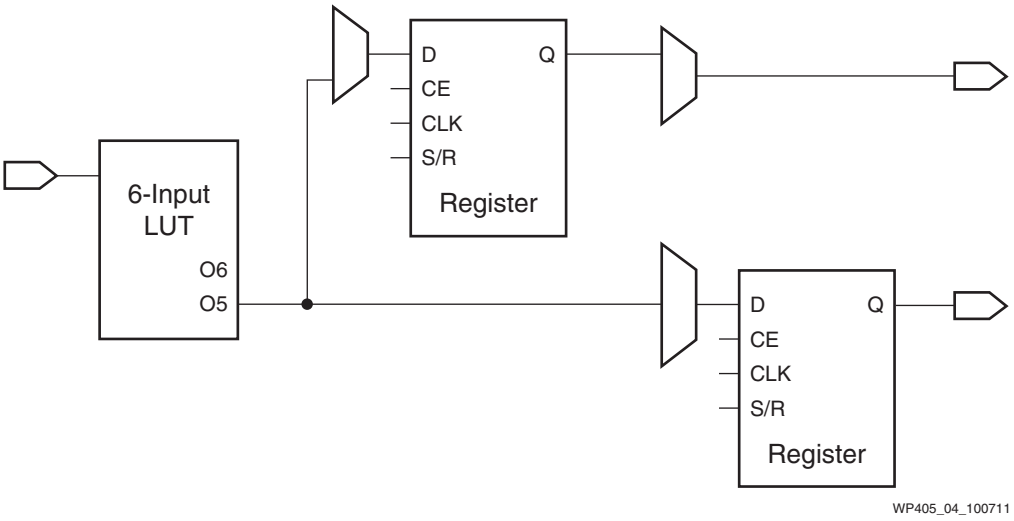

Figure 4: **Using Both Available Registers**

Logical functions that do not share inputs can be created within a single LUT. The A6 input to the LUT is tied High to enable dual LUT mode, leaving the remaining five inputs to the LUT available for independent logical functions. For example, a two-input function and a three-input function that do not share inputs can be packed in the same LUT (Figure 5). If registering the logical outputs, the registers must share the same control signals.

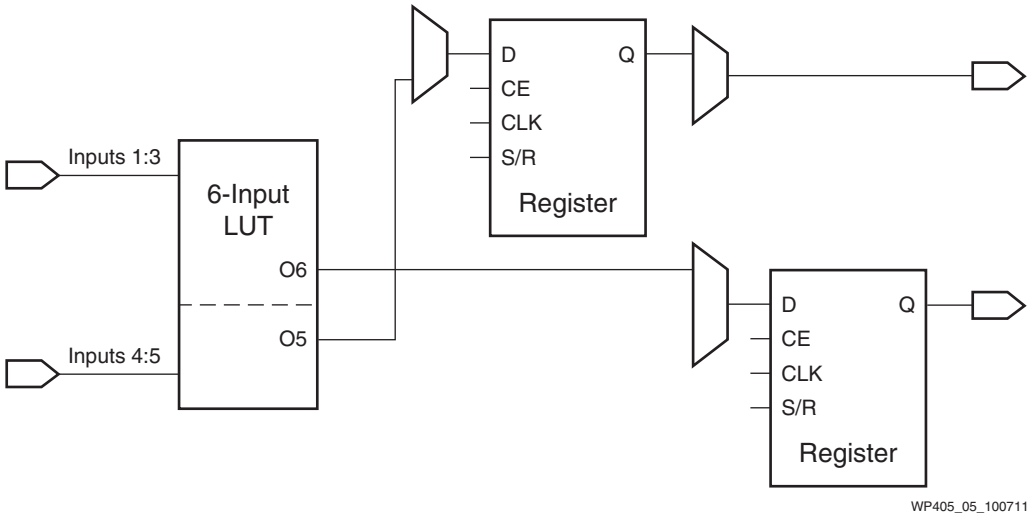

Figure 5: **Two Independent Logical Functions**

The wide multiplexers, F7 and F8, use the bypass inputs to switch between two LUT6 outputs, providing a means of implementing functions wider than six inputs in a single level of CLBs.

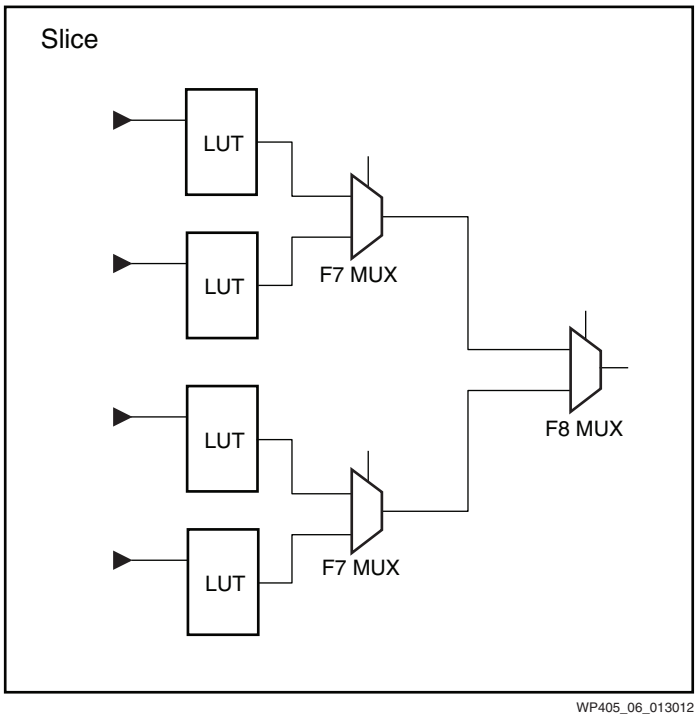

Figure 6: **Wide Logic Functions Using F7 and F8 Multiplexers**

Control Signals

All flip-flops in 7 series FPGAs can be controlled using the set/reset, clock, and clock enable signals, often referred to as a set of control signals or control set. Every slice can use a different control set, but if one flip-flop within a slice uses a control signal, e.g., a synchronous reset, all other flip-flops in that slice must either use the same signal as their reset—or use no reset. It is possible to collapse control signals into the datapath, i.e., the LUT, if there are available inputs to the LUT, allowing more than one reset signal to be used within the same slice (Figure 7).

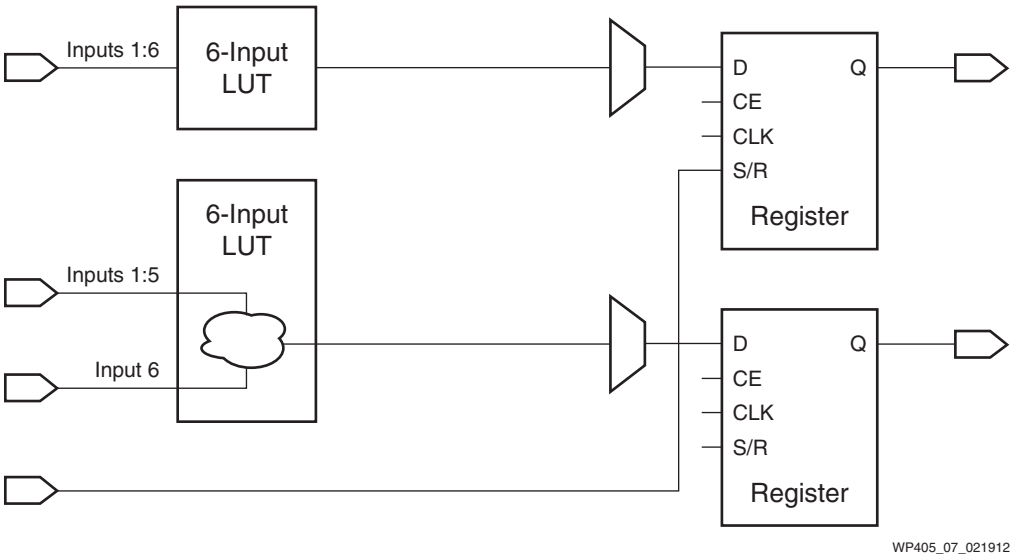

Figure 7: **Two Resets in the Same Slice by Collapsing One into the LUT**

Xilinx recommends avoiding the use of many, low fanout control signals in a design to avoid encountering design limitations due to control set granularity. Synthesis tools automatically avoid generating circuits that use lots of low fanout clock enable signals. In the Xilinx XST synthesis tool, the option "-reduce_control_sets" can be used to control this functionality. UG429, *7 Series FPGAs Migration Methodology Guide* offers further guidance on good design practice with control sets.

All registers can be initialized to a known value on power-up of the device using the initialization value INIT. If the design only requires initialization on power-up, using this method can eliminate the need to have set and reset signals on every flip-flop. This also allows shift registers to be collapsed into the available SRL logic instead of using flip-flops.

In addition to performing user-specified enables, the clock enable ports on the registers are also used by the Intelligent Clock Gating optimization. For more information on how this can help to lower dynamic power of a design by up to 30%, see WP370, *Reducing Switching Power with Intelligent Clock Gating*.

Benefit of Additional Resources

One of the recent changes to the Xilinx CLB architecture is the addition of the second register to the slice. Prior to Virtex-6 and Spartan-6 FPGAs, the CLB architecture in high-end Xilinx FPGAs consisted of four six-input LUTs and four registers. The addition of the second register, which was first implemented in Virtex-6 and Spartan-6 FPGAs and is also present in the 7 series FPGA CLB architecture, adds significant benefits, but it needed to be implemented in a way that had very little impact on overall device cost.

Shown in Figure 8, when configuring the LUT as two five-input LUTs, the outputs of both LUTs can be registered within the same slice. This provides consistent logic to register timing and the ability to register every logical function, thereby aiding performance through pipelining.

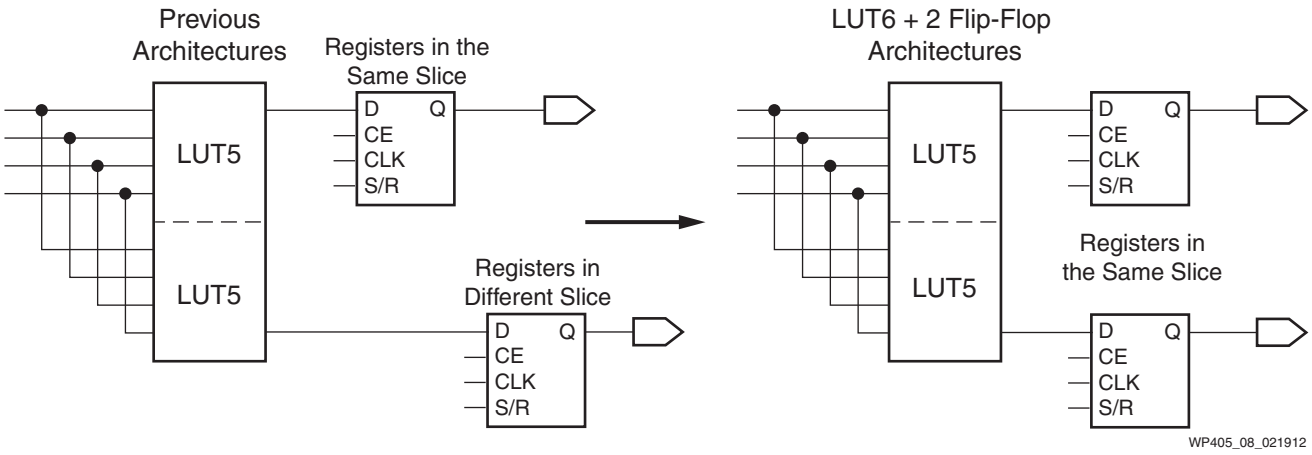

Figure 8: **Two Five-Input Registered Functions**

Additionally, when implementing registered 32 x 8 RAMs out of distributed RAM in a single slice, all eight registers reside within the slice. This eliminates the requirement to use four registers elsewhere in the device, and provides fast, consistent paths from the memory to the registers (Figure 9).

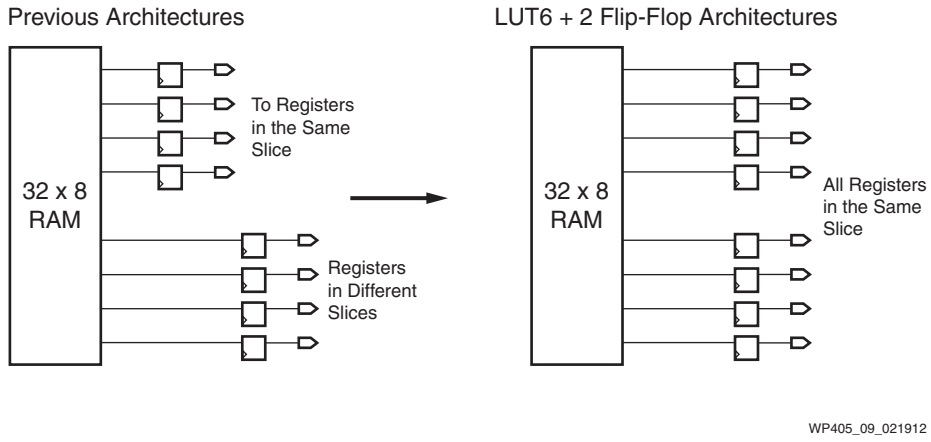

Figure 9: **A 32 x 8 Registered RAM**

The use of all eight registers within a single slice results in a significant performance increase and has the extra benefit of not depleting adjacent slices of their register

resources. The presence of the second register adjacent to each LUT means it is possible to pack more registers that share a control set into a single slice, thereby freeing up resources that would previously have spanned across multiple slices. Analysis over a suite of designs of varying size and complexity shows that this results in an average 15% reduction in slices being used as registers, freeing up resources for the user to build extra functionality into their 7 series FPGA design. Keeping the second register per LUT on the same control set and removing the ability for this register to be configured as a latch means it was implemented and can be leveraged in the FPGA architecture very cost-effectively. While designers can benefit from being aware of the logical architecture when coding their designs, the Xilinx tool suite is aware of the architectural layout of the different families and automatically takes advantage of the resources present in the architecture.

Conclusion

The configurable logic block in Xilinx 7 series FPGAs is an evolution of the CLB present in Virtex-6 FPGAs and Spartan-6 FPGAs, enabling a simple path for designs to migrate into 7 series FPGAs. With four six-input LUTs and eight registers, the flexible slice logic structure can be used to perform many different functions from combinatorial logic functions, arithmetic functions, shift register functions, and memory functions. The combination of four LUTs with eight registers provides both performance advantages and resource reduction over previous architectures, with the low cost implementation of the second register barely impacting overall device cost.

To learn more about how to get the most out of Xilinx 7 series FPGAs, go to the 7 series FPGAs documentation on xilinx.com:

http://www.xilinx.com/support/documentation/7_series.htm

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/06/12	1.0	Initial Xilinx release.

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