



WP408 (v1.0) November 10, 2011

# ***Enabling Next-Generation Broadband Networks over Existing Cable Infrastructure***

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At local cable TV headends that incorporate the computer systems and databases used to originate and communicate cable TV services, multiple system operators (MSOs) are under pressure to deliver more interactive capability and richer triple play data streams. The enabling technology to accomplish this must fit into tighter spaces and consume less power than the legacy equipment it replaces.

Xilinx FPGAs can deliver the increase in silicon device performance required to meet today's video and data specifications, and can be reprogrammed in the field after deployment to meet changes in industry specifications that govern data flows. Built on a 28 nm process technology, 7 series FPGAs deliver a 40% or more reduction in power usage when compared to previous generations, thereby enabling significant performance improvements with the same power budget allocated to previous generations.

## Introduction

After decades of relative stability, traditional cable equipment has rapidly become obsolete due to disruptive technologies like internet protocol television (IPTV) that create new competition for delivering content. This has put MSOs under competitive pressure to increase bandwidth, provide added measures of security, and increase reliability. At the same time, energy costs have increased, real estate and physical headend space have become filled to capacity, and new standards have emerged. MSOs are demanding that their vendors offer smaller, lower power, and flexible equipment to compete. New architectures developed by equipment vendors must be flexible, scalable, and show a roadmap towards lower power. This white paper discusses emerging standards and how FPGAs offer a flexible silicon platform for equipment vendors to meet the needs of a shifting marketplace.

## Specifications Dictate Hardware Changes

In North America, MSOs support the Data Over Cable System Interface Specification (DOCSIS) from Cable Television Laboratories, Inc., (CableLabs). Over the years, CableLabs has addressed the concerns and demands of MSOs by updating the DOCSIS specification. This has led to an increase in security and bandwidth, and a consolidation of cable headend equipment. In the past, however, headend equipment vendors were not able to reuse existing designs and architectures with each major change of the specification. This often resulted in casting new silicon application-specific integrated circuits (ASICs) or application-specific standard products (ASSPs). Often, equipment vendors were forced to absorb development costs for these changes and ultimately, those costs were transferred to the MSOs and their customers. Moreover, equipment vendors were limited by semiconductor/hardware solutions that were neither flexible nor scalable.

Lack of flexibility in silicon devices built on fixed architecture is just one inherent problem with relying on ASICs and ASSPs. The convergence of data and video and the revolution currently taking place in video formats is creating an environment that is moving too quickly for the 18-month development/production cycle required for ASICs and ASSPs. Time-to-market and time-in-market are both addressed by the programmability of FPGAs.

## Combining Voice, Video, and Data

A primary component of the cable headend, the cable modem termination system (CMTS) was first brought to market to provide data and voice over IP (VoIP) service to end customers. The CMTS takes data from the outside network and distributes it to customers through the cable network (downstream). The CMTS is also responsible for accepting data from the customer's cable modem and sending it to its intended destination (upstream). In North America, the downstream frequency range is from 50 MHz to 1 GHz. The upstream frequency range is from 5 MHz to 42 MHz. Furthermore, EdgeQAM modulators were introduced into the cable headend to meet the demand for new and additional video services. EdgeQAM hardware enables video on demand (VOD) and switched digital video (SDV) services.

To address the burden of having to deploy and operate multiple pieces of equipment, CableLabs has recently issued the Converged Cable Access Platform (CCAP) specification. CCAP combines data, voice, and video in a single unit. The CCAP

architecture combines up to 160 QAM channels into a single RF port (F connector) transmitting over the entire cable spectrum from 50 MHz to 1 GHz. The cable headend benefits by having only a single piece of equipment supporting a user group of up to 2,000 homes, with the additional benefit of eliminating the external RF combiner because all the QAM channels are output on a single RF port.

## Meeting Physical Limitations with Flexibility

The latest CableLabs specification, DOCSIS 3.0, does not highlight power consumption concerns for real estate limitations and the ability to reuse existing equipment. The specifications only call for increased bandwidth and higher levels of security and reliability. However, the overall cost for operating a cable plant is also not included in the specification, although this is far from trivial. Costs for powering the cable plant have increased significantly with the explosion in bandwidth, and MSOs are now asking equipment vendors for Watts per QAM benchmarks, a requirement that has moved downstream to silicon vendors.

MSOs are also asking for flexibility regarding CCAP compliant equipment. MSOs have been limited with the ability to upgrade and modify existing architectures after they are deployed in the field. Equipment vendors have provided only limited access to updating the equipment, thus minimizing the effectiveness of these changes. It is not possible to use existing silicon for a newer iteration of the DOCSIS or CCAP specifications. Additionally, this limits MSOs' and vendors' ability to provide proof-of-concept testing, which severely limits the forward progress for the cable industry and the ability to compete with other broadband technologies.

## Inadequacy of Current Hard-Cast Silicon Solutions

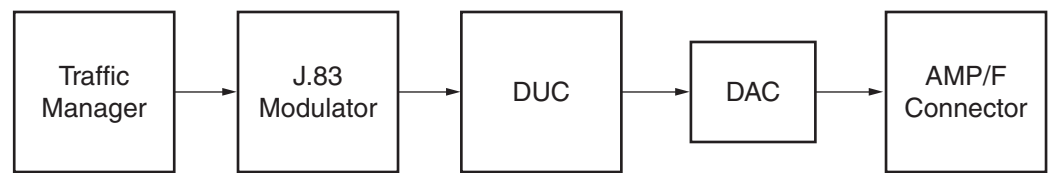
Current silicon solutions for EdgeQAM and CMTS vendors are severely limited in choice, flexibility, and scalability. Each subsequent change in the DOCSIS specification requires a re-architecture of the vendor's hardware. MSOs are forced to purchase new equipment and not take advantage of existing designs. Having the ability to upgrade existing equipment for a proof-of-concept and/or initial testing can speed up development and progress of next-generation networks. As mentioned in [Specifications Dictate Hardware Changes, page 2](#), existing ASIC- and ASSP-based solutions lack flexibility, preventing MSOs from deploying a robust solution in a short period of time.

## FPGAs Meet Evolving MSO Requirements

Ultimately, FPGAs provide MSOs with equipment flexibility, scalability, and a low-power roadmap. Each move to a smaller process node provides an increase in capability along with significant power improvements. Code that is in use today can be ported to next-generation silicon when it becomes available. This provides an instant reduction in power. By moving to a smaller process, more functionality can be included, thereby reducing overall chip count, reducing the bill of materials (BOM), and further reducing the overall board space and board layout complexity. Using an existing code base reduces testing and verification when moving to a new specification.

The 7 series architecture uses a 28 nm process with a power reduction from previous generations. The Kintex™-7 FPGA provides high performance with high density while the Virtex®-7 FPGA provides the highest performance with highest bandwidth connectivity. All 7 series devices are built on state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology. The Kintex-7 family supports up to 478K logic cells, 34 Mb block RAM, and 1,920 DSP slices. The Virtex-7 family supports up to 1,955K logic cells, 68 Mb block RAM, and 3,600 DSP slices.

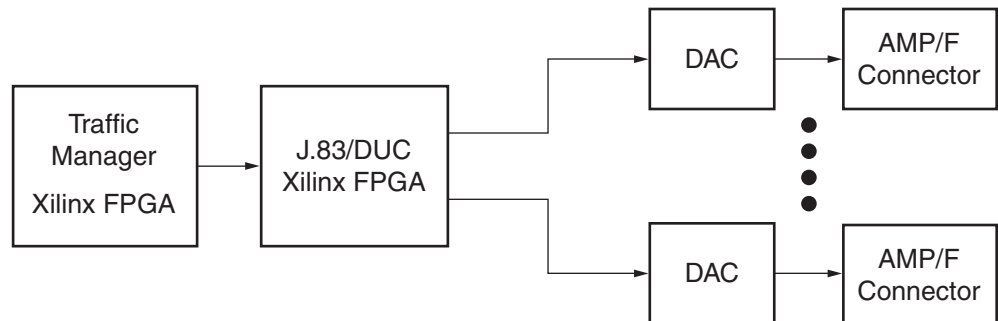
Xilinx has developed several IP cores that can support the latest DOCSIS architecture (Figure 1). Available today are the digital upconverter (DUC), J.83 modulator, and traffic manager. The Xilinx DUC can upconvert up to 160 QAM channels on a single RF port (or F connector). The J.83 core provides the interleaver, Reed-Solomon encoding, randomizer, and QAM mapping. The traffic manager provides packet classification, scheduling, and UDP to QAM mapping.



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Figure 1: DOCSIS Architecture

Customers have the flexibility to interface to a single digital-to-analog converter (DAC) or multiple DACs depending on the application and overall architecture (Figure 2). Cable equipment customers can use existing code to migrate to next-generation designs. The flexibility of the cores allows equipment vendors to use one code base to support DOCSIS, EuroDOCSIS, or J-DOCSIS networks. The correct setting can be configured during the startup procedure. Vendors also have the option of having separate code for each of the three standards, which would be loaded on the system during manufacturing.



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Figure 2: Multiple DACs

Moving the DUC implementation from Virtex-6 FPGAs to 7 series FPGAs provides an estimated power savings of approximately 40%. The increased number of available resources in the 7 series devices allows equipment vendors to include additional IP cores such as the J.83, pre-distortion filters, traffic managers, and media access controller (MAC) functionality onto a single FPGA.

The flexibility of FPGAs also allows equipment vendors to provide a single-chip solution for multiple RF ports. For the CCAP initiative, Xilinx can support a single-chip design with six RF ports. The Virtex-7 VX1140T FPGA has the I/O to

support any high-speed DAC, supporting an RF range of 50 MHz to 1 GHz. The resources of the Virtex-7 VX1140T FPGA support 96 broadcast and 64 unicast QAM channels for each RF port (up to 6 ports), as shown in [Table 1](#). In addition to supporting up to 6 ports in the VX1140T, smaller port counts can be implemented in other 7 series devices, as shown in the table. The flexibility of the Xilinx solution allows equipment vendors to alter broadcast support according to end-user demand. As viewing habits change, MSOs have the ability to reconfigure the broadcast to unicast ratio without having to purchase new equipment or wait for new silicon to be developed. Equipment vendors can simply provide a code upgrade with minimal down time.

**Table 1: RF Port Capability by 7 Series Device**

QAM Channels	RF Ports	Devices
160	1	Kintex-7 K325T
96 Broadcast/64 Unicast	2	Kintex-7 K355T
96 Broadcast/64 Unicast	4	Virtex-7 VX690T
96 Broadcast/64 Unicast	6	Virtex-7 VX1140T

The Xilinx DUC IP core can also be scaled down to support lower QAM channels per RF port. With proven IP cores (J.83, DUC, and traffic manager), equipment vendors can scale down an existing design from 160 QAM channels to 32 QAM channels for smaller broadcasting markets and relevant applications while simultaneously lowering risk and reducing time-to-market. Existing hardware can also be used for proof of concept for next-generation products.

Overall, Xilinx IP cores can support multiple markets with the ability to support DOCSIS, EuroDOCSIS, and J-DOCSIS designs. As an example, the root raised cosine filter roll off or alpha factor can be modified according to the market the code is supporting. Ranges from 18% for 64 QAM or 12% for 256 QAM for DOCSIS can be programmed. If J-DOCSIS is the intended use, 13% can be programmed in (for both 64 QAM and 256 QAM). The EuroDOCSIS alpha factor can be programmed at 15% for either 64 QAM or 256 QAM. The coefficients can be loaded during the power-up stage or selected during system configuration. [Table 2](#) describes the differences in symbol rate, bandwidth, and alpha factor for Annex A, Annex B, and Annex C.

**Table 2: Comparison of Annex A, Annex B, and Annex C**

Parameter		Annex A	Annex B	Annex C
Symbol Rate	64 QAM	6.952 Msym/s	5.056941 Msym/s	5.274 Msym/s
	256 QAM	6.952 Msym/s	5.360537 Msym/s	5.274 Msym/s
Bandwidth		8 MHz	6 MHz	6 MHz
RRC Coefficient	64 QAM	0.15	0.18	0.13
	256 QAM	0.15	0.12	0.13

## IP Bridges to Future Specifications

Cable industry specifications change over time due to new disruptive technologies coming to bear, coupled with changes in end-user viewing habits, increase in competition, or improved manufacturing of supplies and equipment. Headend equipment based on a Xilinx solution incorporates the flexibility to be upgraded in the field with little down time. MSOs can capitalize on existing equipment, while equipment vendors can garner additional revenue by providing new code releases. Moreover, MSOs are no longer forced to purchase new equipment each time a specification is released.

Future headend-based specifications and architectures will incorporate separate upstream and downstream Media Access Controllers while providing Ethernet throughput ranging from 40 Gigabit Ethernet (40GbE) to 100GbE. Another proposed architecture is to provide Physical Layer functionality deeper into the network. Any future scenario fits an FPGA. Equipment vendors can take existing code and demonstrate it on an existing platform with only minor modifications. Furthermore, equipment vendors incorporating Xilinx FPGAs can also take advantage of existing IP cores supporting standard interfaces such as 1GbE and 10GbE. A board redesign can be completed without having to wait for new silicon to be developed. Time-to-market is reduced, and extended verification cycles can be accomplished, thereby providing a reliable system. Xilinx customers have the benefit of using current IP cores for future projects.

## Summary

Cable equipment vendors moving to an FPGA-based solution and architecture inherently adopt a path to an even low-power roadmap. The flexibility and scalability of programmable devices are ideal for proving and verifying next-generation products. FPGAs decrease time-to-market and increase reliability. Most importantly, only Xilinx has an available EdgeQAM, CCAP-oriented solution for cable equipment vendors. Moreover, the DUC, J.83, and traffic manager IP cores not only fit into current headend architecture but can also be part of future solutions. As next-generation silicon becomes available, increasing levels of functionality can be included into more sophisticated designs, further reducing board real estate and complexity. To learn more about how Xilinx FPGAs can meet the needs of MSOs, visit <http://www.xilinx.com/applications/broadcast/edgeqam>.

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/10/11	1.0	Initial Xilinx release.

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