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Unleash the Unparalleled Power and Flexibility of Zynq UltraScale+ MPSoCs

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The Xilinx® Zynq® UltraScale+™ family of MPSoCs provides unparalleled flexibility, dramatically lower BOM costs, and overall project acceleration for complex multitasking designs.

ABSTRACT

Advanced datacenter applications, automotive driver assistance and safety systems, and handheld radio designs all demand scalable SoC IP that can deliver leading-edge performance, while still maintaining high flexibility in the face of varying power availability or conditions.

Application-specific standard products (ASSPs) lock designers into fixed solutions that cannot be scaled. As a result, higher BOM and power costs are forced by the addition of devices needed to support design flexibility.
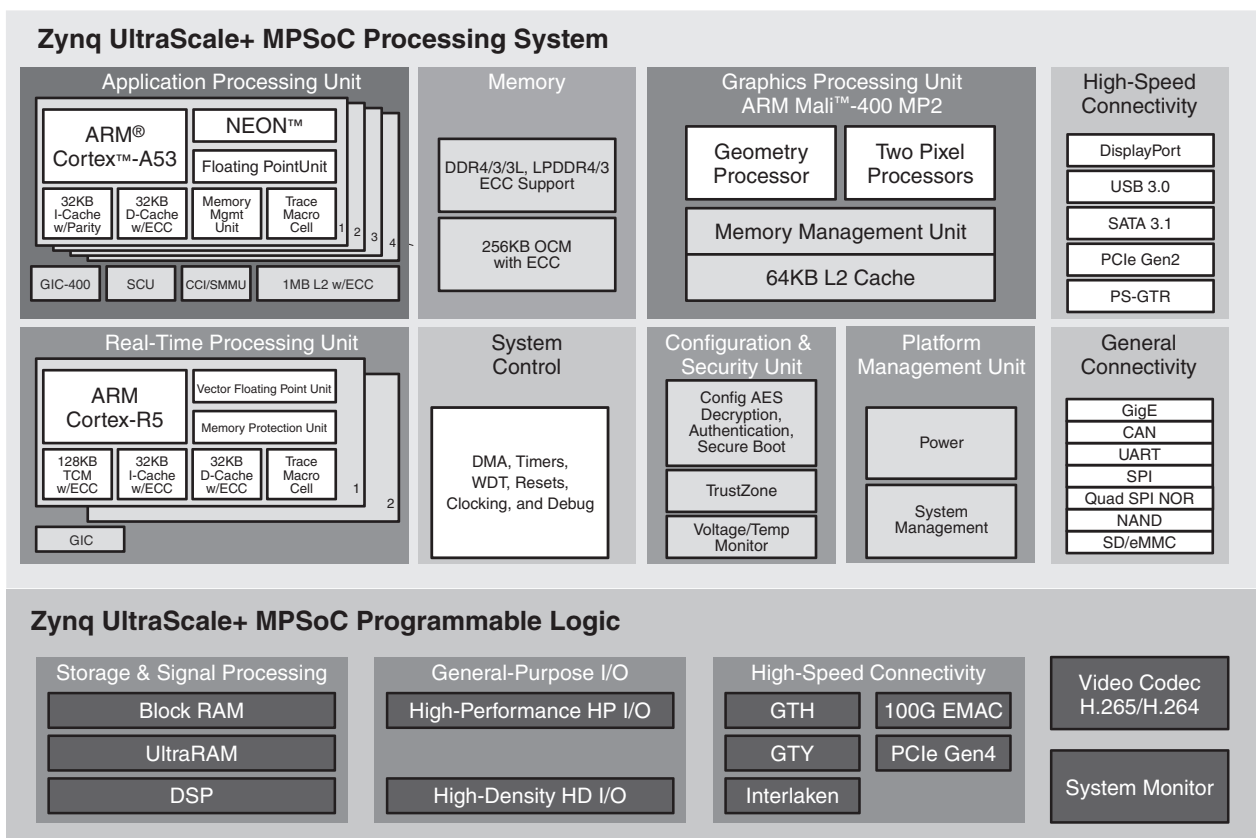
The Zynq UltraScale+ MPSoC delivers new levels of embedded SoC performance with:

- Up to 5X faster system performance per watt (versus the previous Xilinx generation)
- Dramatic new power management features:
  - Integrated power domains
  - Power "islands"
- Advanced video pipeline support at up to 4K with new graphics and video engines
- A proven path to design completion through comprehensive tool and ecosystem support

Introduction

Xilinx introduces the first true all-programmable, heterogeneous, multiprocessing SoC with the Zynq UltraScale+ MPSoC. Built upon the next-generation 16nm FinFET process node from TSMC, the Zynq UltraScale+ MPSoC contains a scalable 32- or 64-bit multiprocessor CPU, dedicated hardened engines for real-time graphics and video processing, advanced high-speed peripherals, and programmable logic serving a wide range of applications like automotive driver assistance and safety, wireless and wired communications, data centers, and connection and control.

Unlike fixed ASSP-based SoC solutions, the Zynq UltraScale+ MPSoC delivers maximum scalability through either dual or quad-core APU devices, and a flexible 32- or 64-bit processing system. It can offload critical applications like graphics and video pipelining to dedicated processing blocks, as well as turn blocks on and off through efficient power domains and gated power islands. With a wide range of interconnect options, DSP blocks, and programmable logic choices, the Zynq UltraScale+ MPSoC has the overall flexibility to fit user application needs. The scalability of the product family can provide designers with the perfect fit for cost-sensitive as well as high-performance applications using a single platform and industry-standard tools.

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Figure 1: **Zynq UltraScale+ MPSoC Block Diagram**

Zynq UltraScale+ MPSoC Processing System Highlights

- Applications Processing Unit (APU) with either quad-core (EG and EV devices) or dual-core (CG devices) ARM® Cortex™-A53 processors:
  - o Next-generation ARMv8 architecture supporting 32- or 64-bit modes
  - o Ideal for Linux and bare-metal SMP/AMP application systems
- Real-time processing unit (RPU) with dual-core ARM Cortex-R5 processors:
  - o Low-latency, highly deterministic performance
  - o APU offloading
- New integrated hardened multimedia blocks:
  - o Graphics processing unit (GPU) [ARM Mali™-400MP2]
  - o 4Kx2K 60fps video encoder/decoder (VCU) [in select devices]
  - o 4Kx2K 30fps DisplayPort interface
- New integrated high-speed peripherals:
  - o PCIe® Gen1 or Gen2 root complex and integrated Endpoint block in x1, x2, and x4 lanes
  - o USB 3.0/2.0 with host, device, and OTG modes
  - o Gigabit Ethernet with jumbo frames and precision time protocol
  - o SATA 3.1 host
  - o Dedicated quad transceivers up to 6Gb/s
- General and boot peripherals:
  - o CAN, I2C, QSPI, SD, eMMC, and NAND flash interfaces
  - o GPIO, UART, and trace ports
- 6-port DDR controller with ECC, supporting x32 and x64 DDR3, DDR3L, LPDDR3, LPDDR4, DDR4
- Integrated platform management unit (PMU) supporting multiple power domains
- Integrated configuration security unit (CSU)
- TrustZone support
- Peripheral and memory protection

Table 1 summarizes the features of the lowest and highest density Zynq UltraScale+ MPSoCs.

Table 1: **Zynq UltraScale+ MPSoC Select Features**

Select Devices	Zynq UltraScale+ MPSoC[1][2]	
	ZU2EG **(Lowest Density Device)**	**ZU19EG** **(Highest Density Device)**
Processing System:		
Multiprocessor APU and RPU Dedicated GPU 6-port DDR memory controller, and on-chip memory Integrated security and platform manager Memory and peripheral port protection plus TrustZone DisplayPort, USB 2.0/3.0 host / device / OTG, SATA 3.1 host PCIe Gen1 or Gen2 x1 / x2 / x4, Gigabit Ethernet CAN, I2C, SPI, QSPI, SD, eMMC, NAND flash GPIO, UART, and trace ports		
Programmable Logic:		
System Logic Cells	103,320	1,143,450
CLB Flip-Flops	94,464	1,045,440
CLB LUTs	47,232	522,720
Distributed RAM (Mb)	1.2	9.8
Block RAM (Mb)	5.3	34.6
DSP Slices	240	1968
Maximum HP I/Os	156	572
Maximum HD I/Os	96	96
GTH Transceiver 16.3Gb/s	0	44
GTY Transceiver 32.75Gb/s	0	28
PCIe Gen3x16 and Gen4x8	0	5
150G Interlaken	0	4
100G Ethernet	0	4

Notes:
1. For full Zynq UltraScale+ MPSoC product information, go to DS891, *Zynq UltraScale+ MPSoC Overview*.
2. See http://www.xilinx.com/products/silicon-devices/soc.html for device availability per family.

Power is Priority

The Zynq UltraScale+ MPSoC has been designed with efficient power management in mind. First, the device is divided into four power domains, as illustrated in Figure 2.
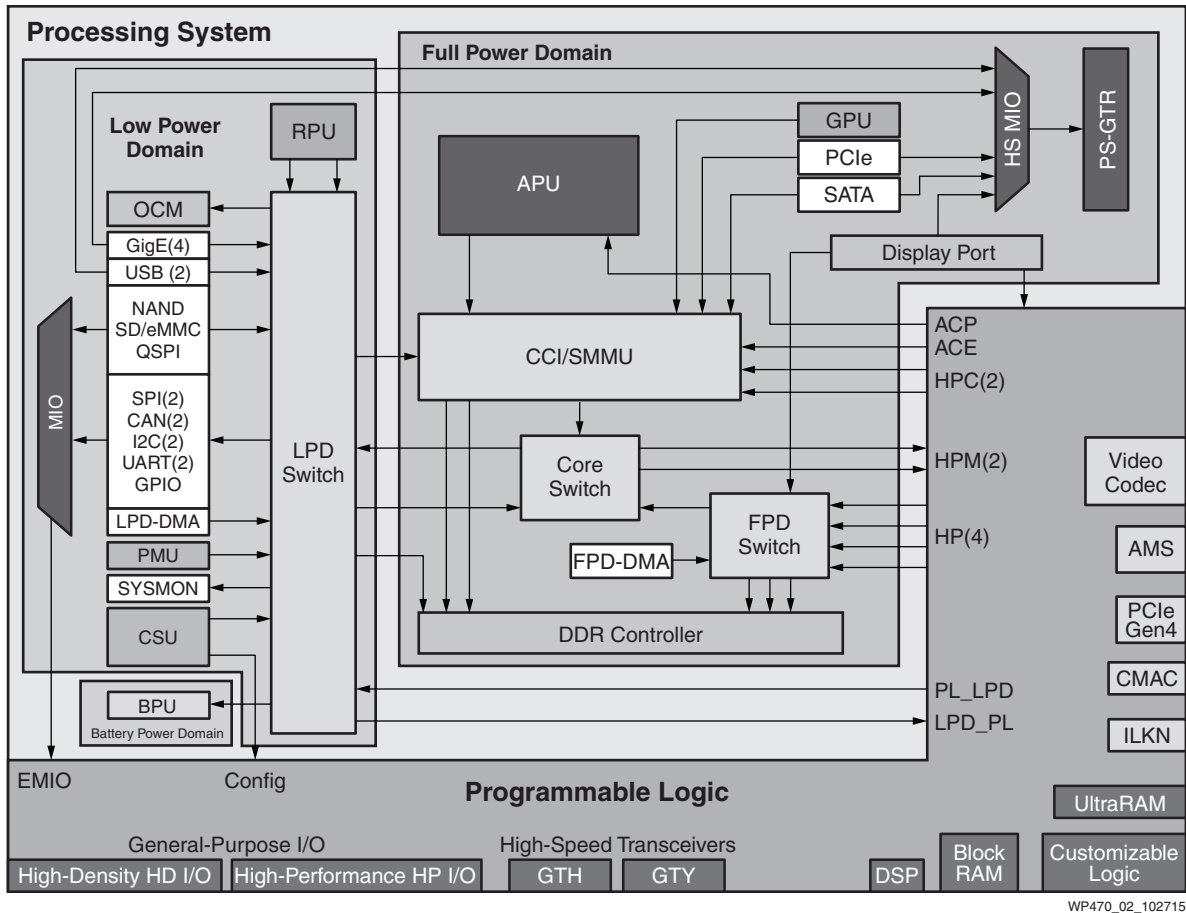

Figure 2: **Zynq UltraScale+ MPSoC Power Domains**

- Battery-power domain in the processing system (PS) containing the real-time clock and battery-backed RAM.

- Low-power domain in the PS containing the RPU, general peripherals, on-chip memory (OCM), platform management unit, and configuration security unit.

- Full-power domain in the PS containing the APU, high-speed peripherals, system memory manager, and DDR controller

- And the programmable logic (PL) is contained within its own power domain

Other than the battery-power domain, which is always on, designers have a wide range of operating modes and power levels to select from. Domains that are not needed can be turned off at boot and then intelligently woken up at an interrupt or event.

The low-power and full-power domains also support power islands on individual engines for even finer-grained control over power. Each Cortex-A53 processor in the APU can be power gated, while the two Cortex-R5 processors in the RPU can be power-gated together, and the pixel and geometry

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processors in the GPU are individually gated. Tightly-coupled memory to the RPU and on-chip memory (OCM) are further broken into banks that can also be individually gated, including the L2 cache in the APU. And many of the general- and high-speed peripherals can also be individually gated as power islands.

Included with the Zynq UltraScale+ MPSoC is an innovative platform management unit (PMU) controlling the power domains. The PMU is responsible for safety management of the device, and governing power within the power domains. It includes a dedicated ROM that handles intelligent domain power-up and power-down, as well as reset requests, and 128KB of RAM for optional custom power management firmware. The PMU includes a 256-bit device key for optional data decryption in a secure restart; it also supports inter-processor interrupts (IPI) so that one domain can watch and wake a sleeping domain at occurrence of a key event.

Up to 5X Greater System Performance per Watt

At the heart of the Zynq UltraScale+ MPSoC are two CPU blocks. The application processing unit (APU) is performance scalable with either dual- or quad-core ARM Cortex-A53s, ideal for Linux and bare-metal applications processing, and the real-time processing unit (RPU) is dual-core ARM Cortex-R5, ideal for low-latency deterministic applications like safety and security modules and APU offloading. Coupled with new multimedia graphics engines, high-speed peripherals, and the latest generation of programmable fabric and IP, the Zynq UltraScale+ MPSoC is able to deliver up to 5X faster system performance over the previous Xilinx generation Zynq-7000 devices.

The ARM Cortex-A53 processors in the APU combine leading-edge performance with power-efficient processing on the ARM v8 next-generation architecture. The APU delivers a baseline 2.7X faster performance over the ARM Cortex-A9 in Zynq-7000 devices, and supports advanced features like next-generation floating-point, and true APM operation through hypervisor support. The APU is ideal for applications-based execution through Linux and other third-party RTOS, or bare-metal execution.

APU highlights include:

- Quad-core (EG and EV devices) or dual-core (CG devices) ARM Cortex-A53 processors
- Up to 1.5GHz operation in the fastest speed grade
- ARMv8 next-generation architecture support
- 64-bit or 32-bit data width operation
- Dedicated memory management unit (MMU) per processor
- Dedicated next-generation, single-instruction/multi-data (SIMD) engine per processor
- 32KB of L1 instruction cache per processor (with parity)
- 32KB of L1 data cache per processor (with ECC)
- Shared 1MB of L2 cache with ECC
- Hypervisor support

The dual-core ARM Cortex-R5 processors in the RPU are optimized for low-latency, deterministic execution, and contain dedicated, low-latency, tightly-coupled memory (TCM) required for safety-critical and high-reliability security applications, or for use as an additional offload processor to the APU.

RPU highlights include:

- Dual-core ARM Cortex-R5 processors
- Up to 600MHz operation in fastest speed grade
- ARMv7R architecture support
- 32-bit data width operation
- Default split-mode operation or dual lock-step operation
- Dedicated memory protection unit (MPU) per processor
- 32KB of L1 instruction cache per processor with ECC
- 32KB of L1 data cache per processor with ECC
- 128KB of low-latency, tightly-coupled memory (TCM) with ECC per processor
- TCM memory can be coupled together to 256KB in lock-step mode

Faster Fabric Performance at Lower Power

The Zynq UltraScale+ MPSoC is built upon the 16nm FinFET process node from TSMC, which features a more efficient transistor implementation with optimal switching speeds and lower leakage current versus planar technology, resulting in greater performance and lower power consumption. Moving from the 28nm-based Zynq-7000 to the Zynq UltraScale+ MPSoC based on 16nm technology yields 60% faster performance at 20% less power.

Available via the UltraScale+ 16nm fabric is high-performance (HP) I/O, supporting up to DDR4 memory speeds; power- and area-optimized high-density (HD) I/O for legacy interfaces; and high-speed serial transceivers, both in the processing system dedicated to high-speed peripherals and in the programmable logic to maximize I/O bandwidth.

Shared system memory is available on-chip with the ability to extend that memory using the programmable logic. External DDR controller interfaces are available both within the processing system, and extended to programmable logic as well, with a new flexible memory map that offers system memory space of up to 16 terabytes.

An Ideal System for Multimedia

New to the Zynq UltraScale+ MPSoC are hardened, integrated multimedia video and graphics processing blocks that operate at up to 4K video rates, letting the CPUs focus on the applications, delivering greater system performance and power efficiency across the device. These new blocks provide a powerful graphics and video management pipeline that can help lower BOM costs by removing extraneous devices from the board.

Graphics Processing Unit (GPU)

The graphics processing unit (GPU) is the ARM Mali-400 MP2 and resides in the Zynq UltraScale+ MPSoC processing system (PS). It is tied directly to the APU and can optionally accelerate the rendering of video images in a frame buffer for display output. The GPU can generate video information through its dedicated, parallel engines much faster than competing ASSPs that rely on the CPU to handle graphics processing, and cheaper and with less power consumption than solutions that rely on the designer to add an off-chip GPU engine.

The GPU accelerates both 2D and 3D graphics with a fully programmable architecture that provides support for both shader-based and fixed-function graphics APIs. It includes anti-aliasing for optimal image quality, with virtually no additional performance overhead. A full set of proven and tested drivers for Linux is included and handles automatic offloading of graphics commands from the APU to the CPU.

Highlights of the Zynq UltraScale+ MPSoC GPU

- ARM Mali-400 MP2

- Up to 667MHz performance in the fastest speed grade

- One geometry processor, two pixel processors

- Dedicated 64KB shared L2 cache

- Dedicated memory management unit

- OpenGL ES 2.0 and OpenGL ES 1.1 support

- OpenVG 1.1 API support

- GPU power gating on each of the three engines

- 1334 Mpixels/sec pixel fill rate

- 72.6 Mtriangles/sec

- 21.34 Gflops floating point shading

Video Codec Unit (VCU)

A new video encoder/decoder is included in the Zynq UltraScale+ MPSoC programmable logic (PL) in select devices. This new hardened codec has access to video and audio streams coming from either the PL or the PS to help deliver and/or access compressed video information by up to 50X over software algorithms, saving valuable system storage space.

Highlights of the Zynq UltraScale+ MPSoC VCU

- Supports H.264 and H.265 HEVC video standards

- Simultaneous encode/decode

- 8K x 4K video at 15fps or 4Kx2K video at 60fps

- 8- and 10-bit color component

- I, IP, IPB frame encoding

- 4:2:0 and 4:2:2 chroma formats

- Up to eight different video streams simultaneously

DisplayPort Interface

The Zynq UltraScale+ MPSoC also includes a new hardened DisplayPort interface module as part of a new package of high-speed connectivity peripherals. The DisplayPort interface is located in the PS and can be multiplexed to one of four dedicated high-speed serial transceivers operating at up to 6Gb/s. This eliminates the need for additional display chips to further reduce system BOM cost.

The DisplayPort interface is based on the VESA V-12a specification and provides multiple interfaces to process live audio/video feeds from either the PS or the PL, or stored audio/video from memory frame buffers. It simultaneously supports two audio/video pipelines, providing on-the-fly rendering features like alpha blending, chroma resampling, color space conversion, and audio mixing. This block also includes a dedicated video PLL for generating synced clocks.

Highlights of the Zynq UltraScale+ MPSoC DisplayPort Interface

- Up to 4K x 2k @30Hz video resolution

- Y-only, YCbCr444, YCbCr422, YCbCr420, RGB video formats

- 6, 8, 10, or 12 bits per color components

- 36-bit native video input interface for live video

- Captured video interface from frame buffers using built-in DMA

- Two-plane rendering pipeline

- Up to two channels of audio, 24-bit at 48KHz

- Dedicated video PLL

- Controller to generate video timing for captured video

- System time clock (STC) compliant with ISO/IEC 13818-1

Application Examples

The scalable power, high performance, and dedicated engines within the Zynq UltraScale+ MPSoC make it ideal for many applications. Some key examples follow.

Data Center: Networked Storage/Service Platform

The majority of websites on the Internet have a SQL database at their core that contains massive amounts of data that need to be rapidly accessible by multiple simultaneous Internet traffic requests. The more popular websites contend with *one trillion page views monthly*, with up to 300 million new photos and videos added every day. However, as websites grow, SQL databases become a bottleneck because they do not scale well. To alleviate this problem, distributed in-memory key-value stores such as Memcached (Mem-Cache-D, a free, open-source, general-purpose distributed memory caching system licensed under the revised BSD licensing protocol) have become critical middleware applications within current web infrastructure. They significantly increase both performance and scalability of web sites by caching the most popular and most recent queries to database.

Memcached is the most widely used open-source software structure to implement key-value stores. The most common Memcached implementation in use today consists of a network adapter and an x86-based motherboard, which uses the host's DRAM memory as the value store. Each unit handles a queued string of database key-value store (KVS) requests. Each request requires decode, hash, read, format, and send steps to be executed. But x86-based architectures do not scale Memcached well—and have already reached performance and power plateaus.

An x86-based Memcached implementation is CPU intensive, and due to random and widely varying key widths, sees frequent interrupts and cache misses that lead to poor branch predictability, stalling of the request pipeline, lower performance, and wasted power. The network adapter layer also adds additional latency through use of a shared TCP/IP stack and through use of data packets to transfer data over DMA to the network adapter. Published benchmarks for multicore x86-based implementations reveal performance numbers of between 5.8–7.0 thousand reads per second per watt (KRPS/W), with latencies of between 200 and 400 microseconds at powers of up to 478 watts per unit.

The Zynq UltraScale+ MPSoC delivers an ideal Memcached architecture by focusing on streaming data from network to memory and back again with very little compute processing. Figure 3 illustrates a Zynq UltraScale+ MPSoC-based Memcached unit architecture. A greatly simplified web server datapath allows each Zynq UltraScale+ MPSoC to saturate a 40Gb/s Gigabit Ethernet link with retrieval traffic. On the data side, the Zynq UltraScale+ MPSoC is driving two banks of NVMe memory via integrated Endpoint blocks for PCIe in the programmable logic. Each MPSoC-based Memcached unit has its own dedicated IP address on the internal network and acts as a stand-alone server, allowing network clients to directly store and retrieve key-value store pairs. Up to 32GB of DDR4 DRAM can be attached directly to the Zynq UltraScale+ MPSoC PS, with expansion DDR memory available through the Zynq UltraScale+ MPSoC PL. As much as 100GB/s of DRAM access bandwidth is available.
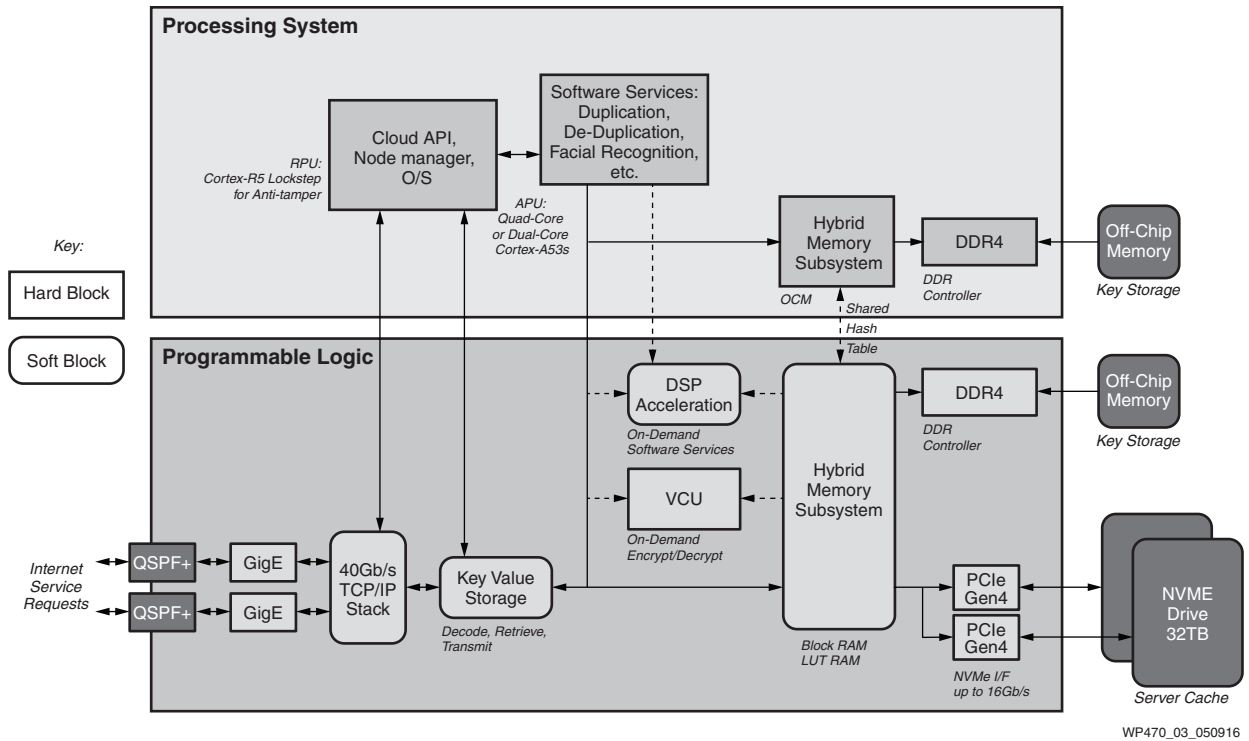
Figure 3: **Zynq UltraScale+ MPSoC Data Center Example Application**

All of the Key-Value Storage processing is located in the MPSoC programmable logic, including the MAC PHYs, eliminating the need for additional BOM parts, and lowering overall system power. All the core systems can be driven directly from programmable logic including two 40Gb/s network lines for the Gigabit Ethernet blocks, TCP/IP stack processing, DDR4 memory control, and dual NVMe PCIe interfaces handling up to 32TB of cache memory.
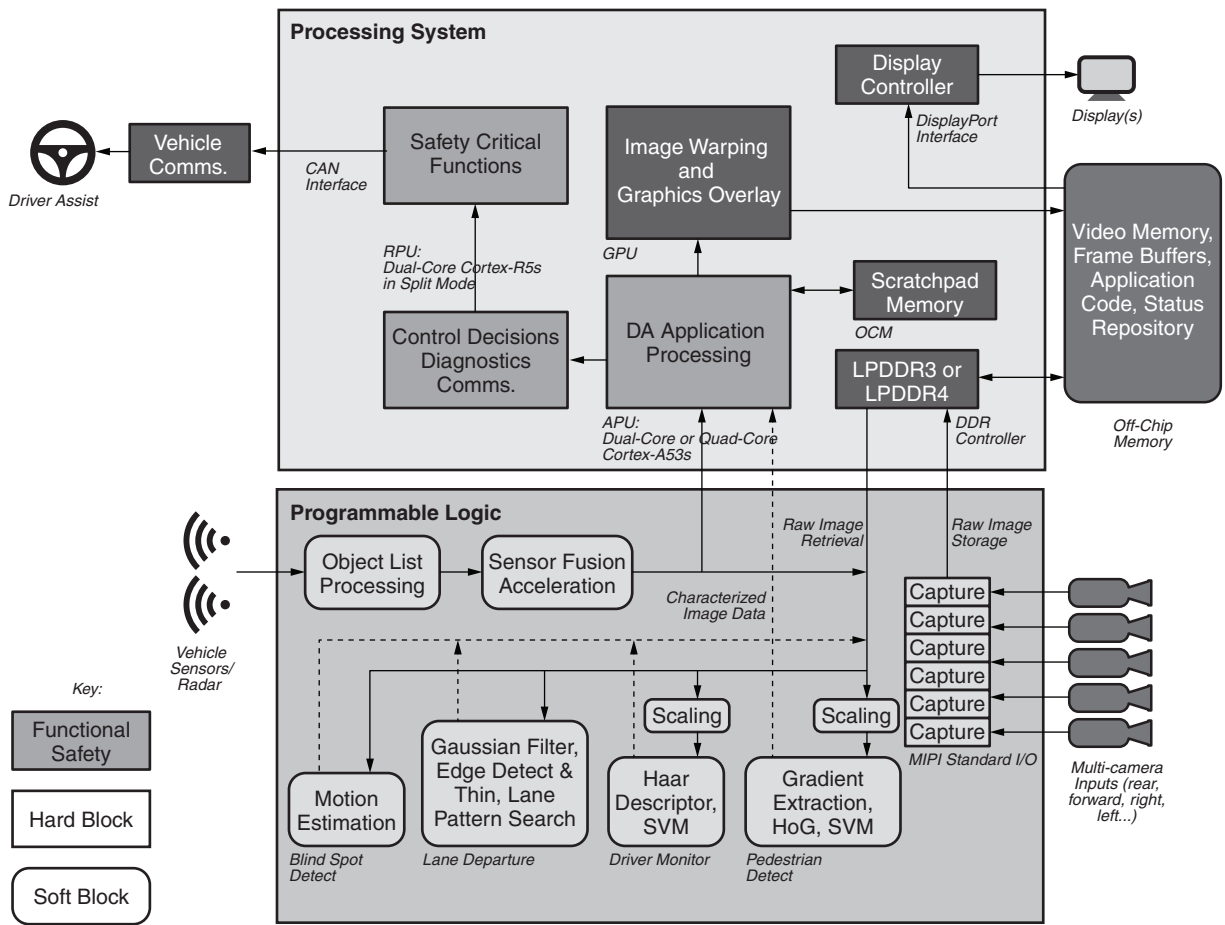
And the MPSoC delivers additional functionality, like dual compression and decompression of data using the integrated VCU. The APU can be used to run control plane software for a multi-tiered blade farm, or alternately run Open Storage Platform management software like Kinetic, eliminating the need for additional control modules. Each APU processor running a Linux OS and coordinated through a hypervisor can separately provide software-defined services such as data duplication, search, analytics, or image recognition and enhancement.

The MPSoC delivers dual QSFP+ line rates of up to 80Gb/s of key-value storage where the web server becomes the pipeline bottleneck, and up to 32TB of storage. Performance now can reach an estimated 104MRPS or a 4.5X performance speed-up over x86 implementations, at 27 watts, or a 20X power reduction.

Zynq UltraScale+ MPSoC in the Vehicle: Central ADAS Module

Zynq-7000 devices are already commonly used in vehicle safety and camera systems in vehicles on the road today. The number of camera systems in vehicles is expected to double within the next four years, including stereo ranging. The car's central ADAS unit is expected to handle video pipelines with up to six simultaneous cameras at a minimum of 2 megapixels at 30fps each, a requirement that the Zynq UltraScale+ MPSoC is ready to meet.

Figure 4 illustrates this example application.

Figure 4: **Zynq UltraScale+ MPSoC ADAS Example Application**

With the Zynq UltraScale+ MPSoC in the ADAS central module, the device's I/O handles video link capture from multiple cameras throughout the vehicle using various interface standards including MIPI and Ethernet protocols. Raw video is then passed to video and analytics IP running in the PL, supporting accelerated functions like motion estimation for blind spot detection, headlight/taillight classification for headlamp control, edge-detection for lane departure warning, pattern recognition and optical flow estimation for traffic sign recognition, and gradient extraction for pedestrian detection.

The processed image data is then fed to the Zynq UltraScale+ MPSoC processing system, where the APU quad-core processors perform environmental characterization of the image data while simultaneously monitoring vehicle sensors. The APU can adjust the hardware accelerators in the

programmable logic by setting parametric control registers, like thresholds for edge detection, or dynamically switch module loading from lane detection to monitoring pedestrians while sitting stationary at a traffic light. The APU performs frame-based processing, like object tracking and range estimation. Any additional video processing like warping to correct for camera lens shape gets offloaded to the GPU leading to better CPU performance and more even thermal balancing.

Information characterizing the vehicle environment is sent from the APU to the RPU. The RPU functions as the primary interface to the vehicle for monitoring and initiating actuators while performing system diagnostics in parallel. The dual-core Cortex-R5 processors run in lock-step mode to meet functional safety requirements. Commands to the vehicle are sent from the RPU via integrated CAN interface, with potential cross-monitoring and diagnostic-protected voting in the programmable logic.

The APU and RPU together provide ADAS host controller integration with functional safety support. In addition to these processing units, the input video links, graphics processing, integrated CAN interface, and programmable logic for hardware acceleration are all included onboard the Zynq UltraScale+ MPSoC, reducing overall BOM costs, eliminating the need for a separate host controller and camera video link interface, plus integrating GPU and onboard memory to lower the overall system power of the ECU by up to 25%. This leads to a 4X performance-per-watt advantage over a similar implementation using Zynq-7000 AP SoC architecture.

Zynq UltraScale+ MPSoC over the Airwaves: Software-Defined Radio

The need for power-sensitive performance dominates the mobile radio market. In both land mobile radio (LMR) and professional mobile radio (PMR), the overwhelming trend is for software-defined baseband architectures that deliver multiple wideband modulation schemes (LTE, TETRA), and even simultaneous multiple modulation schemes in next-generation products. The need is for radio platforms to host data applications optimized for public safety or private networks. The Zynq UltraScale+ MPSoC family is ideally suited for the public radio market.

A battery-powered narrowband public safety radio spends up to 90% of its time in standby mode, with the remaining 10% operating transmit/receive. A Zynq UltraScale+ MPSoC software-defined radio takes advantage of the integrated power domains and power islands within the MPSoC to shut down all unused systems. The monitored waveform from the input RF module is continually monitored by one of the Cortex-R5 processors in the RPU, while the other Cortex-R5 handles security. The full-power domain, including the APU and programmable logic, remain shut down, with the entire system drawing as little as 35mW.

Figure 5 illustrates how the Zynq UltraScale+ MPSoC family can be leveraged to simplify implementation of these requirements.
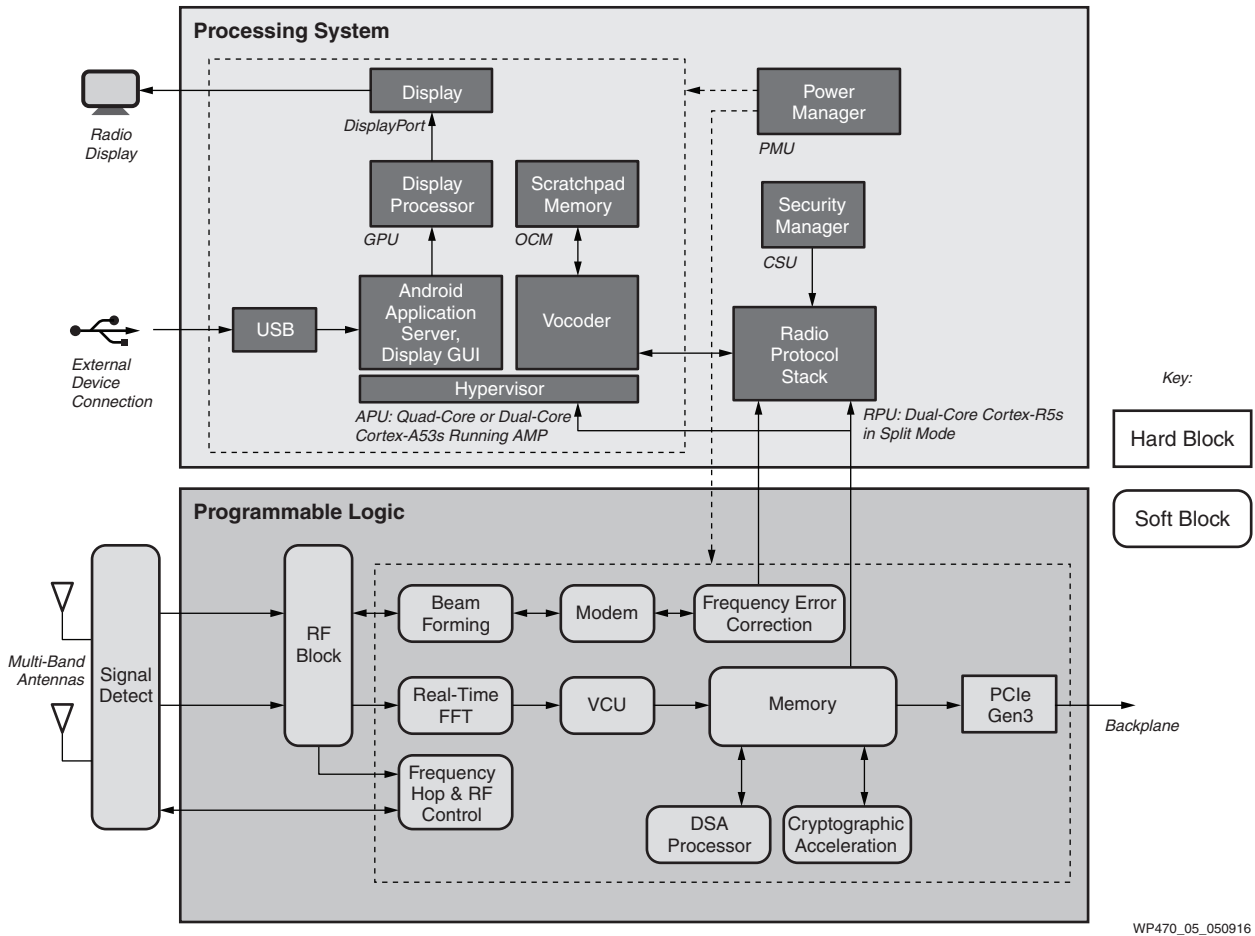

Figure 5: **Zynq UltraScale+ MPSoC Public Radio Example Application**

Upon detection of a valid transmission, the RPU wakes up both the APU and the programmable logic via inter-processor interrupt. The programmable logic then immediately begins handling RSSI authentication, filtering, and packet header decryption. After the transmission is authenticated, one Cortex-A53 processor in the APU begins Vocoder processing, taking advantage of its integrated next-generation SIMD for the fastest possible performance. Simultaneously, a second Cortex-A53 has woken up the display. Additional android-based applications can be served through the remaining two processors (available in EG and EV devices). The APU processors can be run completely asymmetric via a hypervisor, and can be gated off when not in use via power islands. The integrated VCU is also available for encryption/decryption and offline storage of signals if needed.

With the diversity of the multiprocessors and hardened engines available in the Zynq UltraScale+ MPSoC, the RPU continually monitors and watches for an applicable signal, keeping the remainder of the power domains asleep at considerably lower power consumption. With the improvements made in the programmable logic and new lower power memory interfaces, the Zynq UltraScale+ MPSoC can achieve close to a 5X performance-per-watt improvement versus existing software-defined radio implementations.

Conclusion

Choosing the right embedded platform for a next-generation project does not have to confine the user to restrictive ASSP SoCs. The Zynq UltraScale+ MPSoC delivers true multiprocessor hardware and architecture flexibility, with fine-grained power control through multiple power domains and gated power islands, coupled with the dedicated high-performance engines needed to tackle multimedia pipelining. All family members include a scalable range of programmable logic for custom accelerators, a range of high-speed and general-purpose I/O, and an optional VCU that can keep BOM costs down.

For more information on Zynq UltraScale+ MPSoCs, go to:
www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/15/2016	1.1	Updated Introduction; Figure 1; Zynq UltraScale+ MPSoC Processing System Highlights; Table 1; Up to 5X Greater System Performance per Watt; Figure 3; Figure 4; Zynq UltraScale+ MPSoC over the Airwaves: Software-Defined Radio; and Figure 5.
11/06/2015	1.0	Initial Xilinx release.

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