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# All Programmable RF-Sampling Solutions

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*The integration of direct RF-sampling data converters with Xilinx's All Programmable technology offers the most flexible, smallest footprint, and lowest power solution for a wide range of radio applications.*

## ABSTRACT

To achieve the performance required of the latest generation of wireless access, DOCSIS, and a plethora of other radio applications, direct RF-sampling technology holds the promise of increased flexibility and higher performance. Direct RF-sampling provides the flexibility by moving much of the RF signal processing into the digital domain, thereby eliminating much of the analog signal processing[Ref 1][Ref 2].

However, there is immense market pressure to reduce the power and footprint of these systems. The solution is to integrate RF-sampling data converters with VLSI devices using advanced CMOS technology.

Xilinx® All Programmable technology has long provided a highly flexible digital signal processing solution for a range of radio applications[Ref 3][Ref 4]. Integrating direct RF-sampling data converters enables a highly flexible platform for radio development that also addresses many of the challenges associated with current direct RF-sampling solutions.

# Challenges for Next-Generation Radio Systems

Meeting the challenges of future wireless access[Ref 5], DOCSIS, and instrumentation involves significant changes to existing radio architectures. New architectures will leverage the latest innovations to better utilize existing spectrum and improve the capacity of networks using techniques like carrier aggregation (CA)[Ref 6], massive MiMO[Ref 7], and digital beam forming (DBF) to implement adaptive arrays[Ref 8].

The cost associated with moving data between these new RF front ends (RFFE) and the digital front end (DFE) is one of the key challenges that must be resolved to make these new technologies commercially viable. Another key requirement is increased flexibility and programmability of the RFFE to reduce time to market and provide a platform that addresses the wide range of emerging next-generation radio requirements.

## The Increasing Bandwidth Problem

The Shannon-Hartley theorem defines the amount of information that can be transmitted over a wireless channel, as shown in [Equation 1](#):

$$C = BW \times \log_2 (1 + SNR) \quad \text{Equation 1}$$

Simply stated,  $C = B \times \log_2 (1 + SNR)$  where  $C$  is the capacity,  $B$  is the signal bandwidth, and  $SNR$  is the signal-to-noise ratio in the channel. The information capacity ( $C$ ) is directly proportional to the bandwidth ( $BW$ ) of the channel. With the amount of data being transmitted over mobile wireless networks increasing by approximately 50% every year[Ref 9] and forecast to reach 30 exabytes by 2020, the demand for bandwidth is also increasing at pace.

The same bandwidth pressure exists in other networks using similar radio technologies, like DOCSIS 3.1. New cable architectures like remote PHY (R-PHY)[Ref 10], and the move to fully digital optical networks enables fully symmetrical residential data rates >1Gb/s.

In all these use cases, the basic radio must be able to support very wide bandwidths. For mobile communications in the sub-6GHz bands, RFFEs must support up to or exceeding 400MHz of signal bandwidth for carrier aggregation, and also address wider contiguous bandwidth allocations becoming available above 3GHz. On transmit and observation feedback paths used for digital pre-distortion (DPD), bandwidths over 1GHz must be supported to linearize the RF power amp (RFPA). Similar bandwidth requirements are needed to support emerging fully symmetrical DOCSIS standards, as mentioned previously. For data converters sending large amounts of sampled data to and from the DFE for processing, multi-gigabit sample rates on the I/O interfaces must be supported.

[Figure 1](#) illustrates the high power cost of simply moving the data from a wideband (1GHz) 2x2 RFFE into the DFE for processing using discrete RF-sampling data converters. Even with integrated digital down-conversion (DDC) or digital up-conversion (DUC) in the data converters, large amounts of data still need to be sent to and from the DFE. The I/O power number shown for each quad transceiver (1W per, four lanes) includes the power associated with implementing the JESD204 protocol on the latest All Programmable 16nm devices from Xilinx.

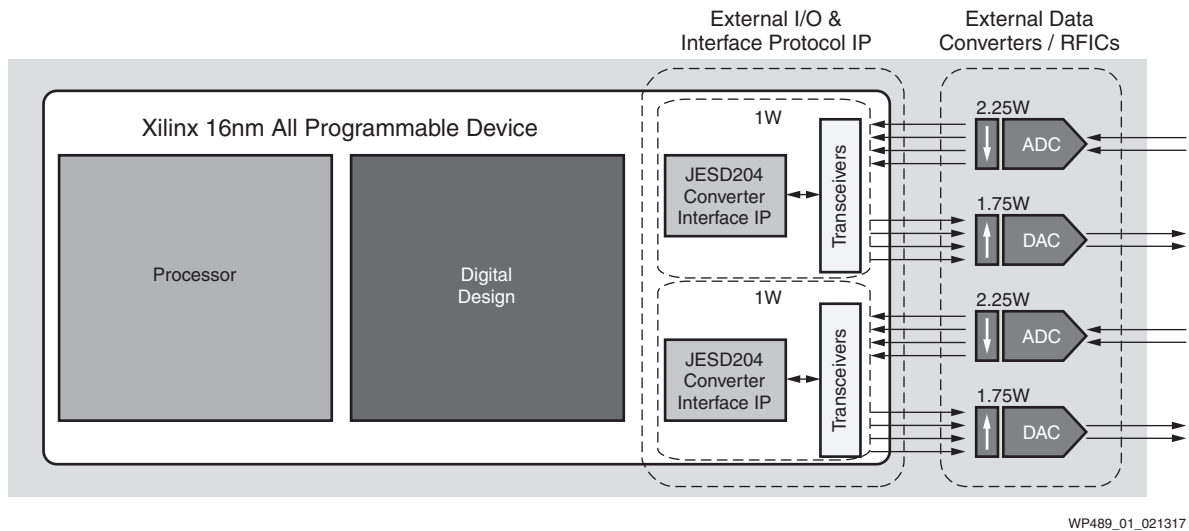


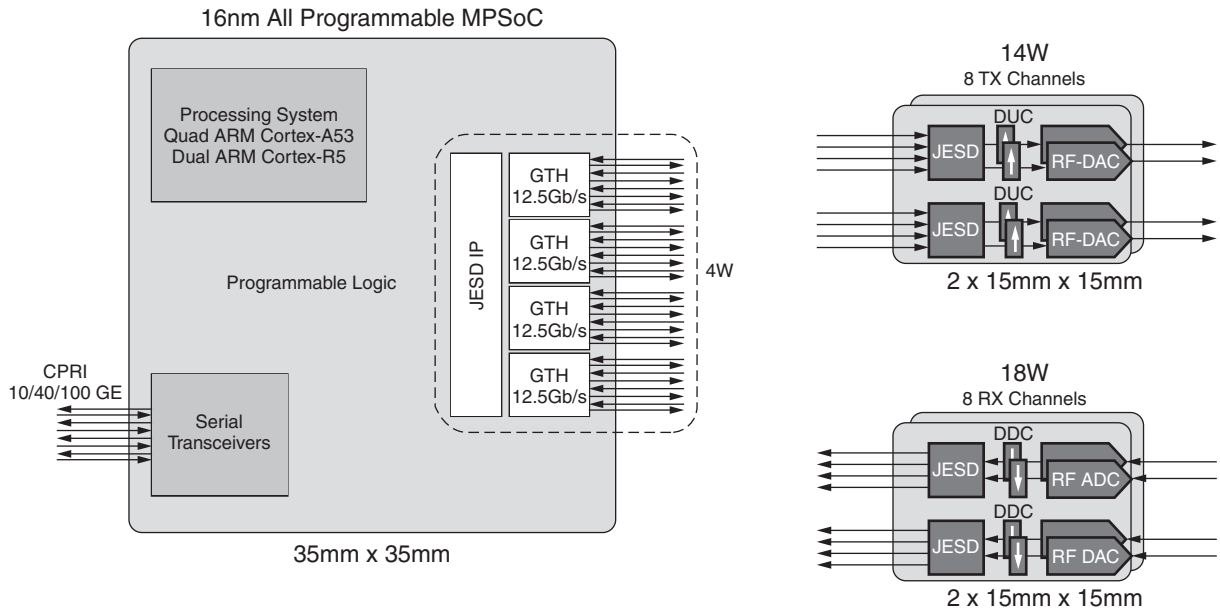
Figure 1: Interfacing to External Wideband Data Converters Using JESD204

In addition to the power of the interface, the power consumption of the high-sample-rate converters also needs to be addressed to lower overall system power consumption. The power of external giga-sample data converter solutions remains stubbornly high. DFE signal processing has leveraged the latest deep-submicron CMOS technologies to reduce power, while RF and other analog components have traditionally leveraged older-process technology. The older CMOS and even BiCMOS technology offered the required performance at the right costs for these predominately analog (“Big A”) discrete components. However, as described in [Moore Digital is the Key](#), the move to a more digitally dominated SoC (“Big D”) means that it is now commercially viable to build data converters on the latest advanced CMOS technologies, allowing huge power and cost savings.

## Increasing Antenna Counts

The Shannon-Hartley theorem refers to the bandwidth of the channel as the biggest driver of wireless channel capacity. The other limiting factor is the signal-to-noise ratio (SNR) in the channel. A promising technique that can dramatically improve SNR and thus the capacity of the channel is the use of active phased arrays. This technique is sometimes referred to as *array gain* and involves the use of a large number of antennas to effectively boost the signal and minimize interference or noise. The higher antenna count can also be used to increase the capacity of the channel using MIMO techniques. This effectively increases the bandwidth without the need to allocate more spectrum[Ref 11].

Figure 2 illustrates the challenge of deploying direct RF-sampling using discrete converters in an 8-antenna system. The move to RF-sampling has already reduced the footprint by removing the analog components typically found in heterodyne radio[Ref 12]. However, for the 8T8R implementation shown, the interfacing alone (in terms of power and PCB routing) is cost-prohibitive for many applications.



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Figure 2: Interfacing of a 8x8 RFFE to the DFE

The implementation shown in Figure 2 assumes an integrated four-channel RF-sampling ADC or DAC in a single 15mm x 15mm package. This integration helps reduce the footprint of the discrete data converters; however, it does little to reduce the complexity or power of the interface. In fact, the integration of more converters into a single package can add additional layers to the PCB to route a high number of serial transceiver lanes to a more localized area on the PCB. In the example, up to four watts of power are dissipated just to move data between the DFE and RFFE. Again, as in Figure 1, the power cost of a single quad transceiver plus JESD204 IP is approximately 1W.

## The Need for Ever-Increasing Flexibility

Future radio architectures will need platform technologies that can address a wide range of requirements with the same basic hardware. The ability to leverage the same hardware to address diverse requirements and emerging standards allows vendors to react quickly to new market opportunities. In the case of 5G systems, for example, it is becoming clear that no one type of radio will address the diverse needs of next-generation radio access networks (RANs). Consequently, the number of different radio types can be expected to increase significantly [Ref 13].

Xilinx's All Programmable SoCs and FPGAs have provided very flexible solutions for implementing the DFE and interfacing requirements for recent radio generations. The same level of flexibility and programmability must be pushed closer to the antenna in the next generation of radios to move towards the goal of software-defined radio (SDR). Direct RF-sampling, integrated with highly optimized RF digital signal processing engines (i.e., DDC and DUC), offers a much more flexible approach to traditional analog frequency translation and filtering. By leveraging advanced CMOS technology, RF signal processing, with excellent power and cost efficiency, can be implemented in the digital domain. As a result, the RF-sampling solutions deliver a very flexible RF front end with the ability to deal with very wide bandwidths—up to 2GHz—at a much lower power draw than required by analog technologies. By pushing data converter sample rates very high, much of the

application-specific analog filtering and signal conditioning can be moved closer to the antenna, thus moving closer to Mitola's vision of a fully software-defined radio [Ref 14], as shown in Figure 3.

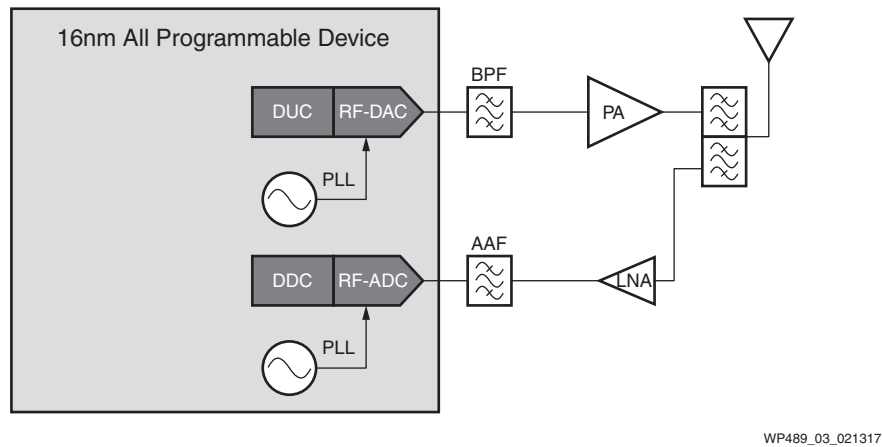


Figure 3: Software Defined Radio Using Direct RF-Sampling

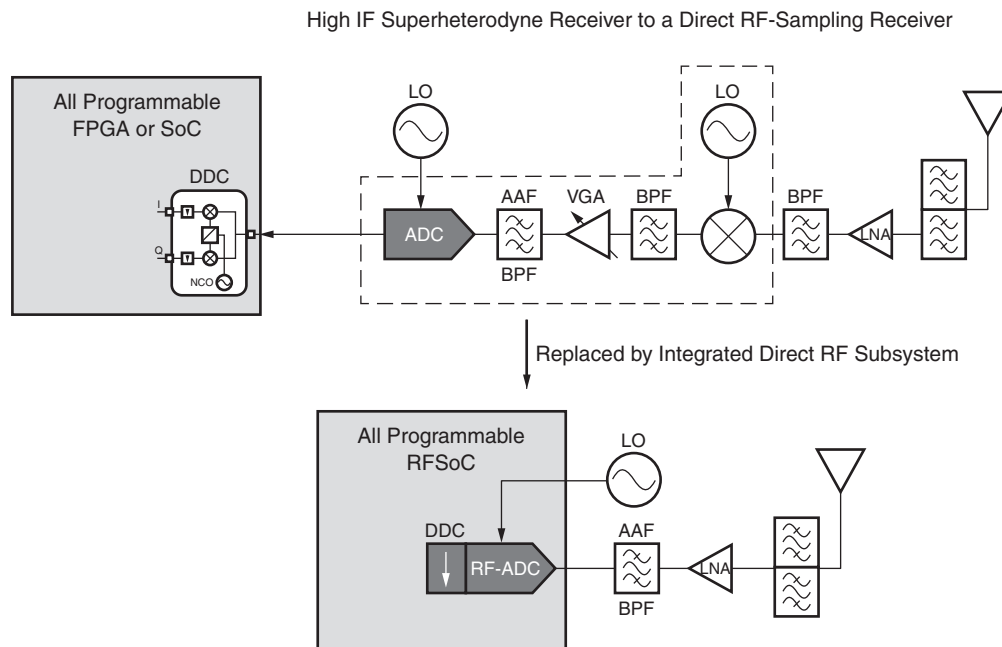
## Moore Digital is the Key

Direct RF-sampling data conversion enables the application of Moore's Law to analog. It allows analog/RF signal processing to be moved into the digital domain, where advantage can be taken of advanced CMOS technology; the same functionality can be then delivered in a much smaller area at lower power [Ref 1]. Advanced FinFET process technologies are enabling new digitally assisted analog techniques that greatly improve the power efficiency of these circuits versus complex analog components [Ref 15].

The integration enabled by these technologies addresses the key challenges of power reduction and increasing channel counts. Also, by moving much of the signal processing into the digital domain, the path to a more flexible or programmable solution is realized. Xilinx's All Programmable FPGAs and SoCs have provided a uniquely flexible radio development platform for a number of generations [Ref 3]. As such, Xilinx devices are a natural platform for the integration of direct RF-sampling data converters.

## Advantages of RF-Sampling ADCs and DACs

Other direct RF-sampling benefits include the reduced complexity of the RFFE (see Figure 4). The higher sample rates supported by these RF-ADCs and RF-DACs greatly simplifies the analog filtering requirements and also allows a better trade-off between dynamic range (SNR) and signal bandwidth in the digital domain by decimating and filtering the ADC output to extract only the signal bandwidth of interest [Ref 1]. The large unused portions of the Nyquist bandwidth of the converter can also be used to inject band-limited dither to improve the converter linearity. Implementing the signal conditioning in the digital domain also yields better performance and ease of use. Some of the traditional RF impairments in the intermediate frequency (IF) approach are greatly reduced or eliminated, e.g., passband ripple, group delay variation, matching, local oscillator (LO) leakage issues, etc.



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Figure 4: Comparison of Superheterodyne and Direct Sampling Receivers

A widely used metric of converter performance is the effective number of bits (ENOB). It is often cited to suggest that lower sample rate converters or using the data converters in the first Nyquist zone with IF or zero intermediate frequency (ZIF) architectures is the optimal approach from a receiver performance and power efficiency point of view.

However, ENOB can be misleading. It is much more useful to evaluate the noise spectral density (NSD) of the converter. For example, the ADC full scale NSD is a better measure of the receiver blocker tolerance and dynamic range [Ref 16]. The problem with ENOB is that it combines noise and all distortion artifacts into a single metric. But these non-idealities affect receivers in different ways and thus need to be treated separately [Ref 17].

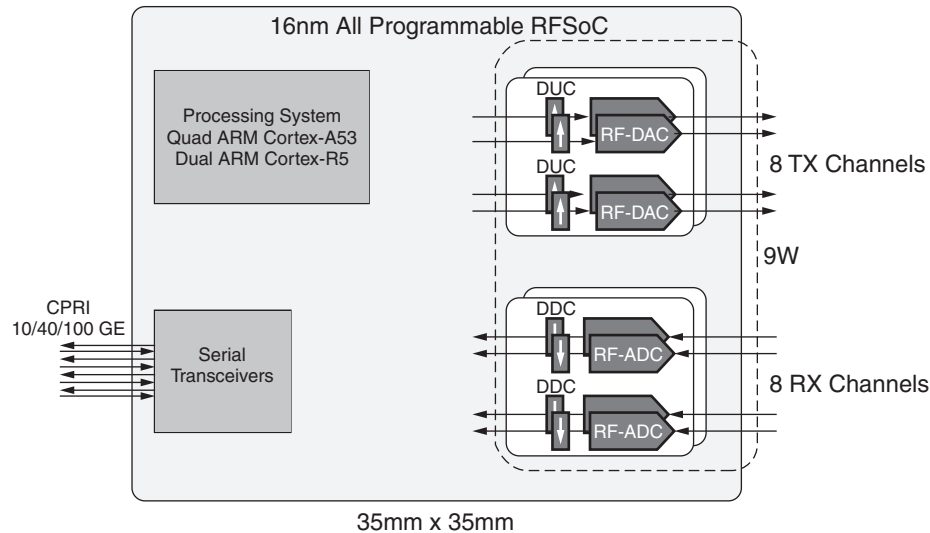
## A Fully Integrated RF Signal-Processing Front End

The integration of direct RF-sampling ADCs and DACs into Xilinx's All Programmable devices addresses many of the challenges associated with current SDR platforms based on ZIF or heterodyne architectures. The Xilinx devices offer a feature-rich platform that includes DSPs, general purpose processor (GPPs), programmable logic, and optimized RF signal-processing blocks (i.e., DDCs and DUCs).

While the primary goal is to provide a more flexible (software programmable) radio, the integration also eliminates the need for external I/O interfaces, which can consume a significant amount of power, as shown in Figure 1. Eliminating external I/O also removes:

- A significant bottleneck in existing SDR solutions [Ref 18].
- The large number of clocks needed to drive the JESD204 interfaces.
- The complexity of routing the clocks on the PCB and synchronizing all the links.

The elimination of the external interfaces also greatly reduces system power. Recent direct RF-sampling implementations on the latest CMOS technology have also been shown to produce very favorable benchmarks in terms of power and cost when compared to traditional integrated heterodyne implementations[Ref 16]. Figure 5 shows how the RF-sampling converters can be implemented in 9W versus 36W using discrete solutions.



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Figure 5: All Programmable RF Front End

It is clear from Figure 5 that the impact this level of integration brings is very disruptive when compared to Figure 2. The integration of a large number of converters enables the deployment of increased channel counts within a much smaller footprint, enabling many of the advanced transmission technologies like massive MIMO and digital beam-forming described in Challenges for Next-Generation Radio Systems to become commercially viable. The integration of the RF-sampling data converters has reduced the footprint of the DFE and converters by ~50%.

### Implementing High Performance Data Converters in 16nm FinFET Technology

In recent years, significant developments have been made in high-performance analog design built on advanced CMOS technology. Xilinx has delivered high-speed serial state-of-the-art transceiver designs in the latest CMOS technology for a number of years by leveraging advanced digital techniques.

Most recently, Xilinx has been delivering 32Gb/s backplane-capable transceivers at 16nm. Other innovations were outlined at the International Solid-State Circuits Conference (ISSCC). In February 2017, Xilinx presented its achievements in direct RF-sampling converter performance in the 16nm FinFET process from TSMC. Two conference papers describing a 13-bit 4GSPS RF-ADC[Ref 19] and a 14-bit 6.8GSPS RF-DAC[Ref 20] were presented in the Gigahertz Data Converters session. The power dissipation cited is 500mW and 330mW, respectively. Impressive levels of performance in terms of NSD and distortion clearly demonstrate a compelling argument for direct RF-sampling on a “Big D” process node.

## A Comprehensive Platform for Radio Development

The silicon, while important, is only half of the platform solution. A fully integrated tool flow for the design and verification of the radio solution is critical. Xilinx offers a comprehensive tool flow that encompasses logic design, embedded SW development, and simulation.

RF-sampling solutions need to be supported by verified and tested IP along with the required software drivers that allow developers to focus limited resources on innovation and differentiating features for the end product. The development environment allows the reuse of IP and subsystems across multiple designs and design teams.

For an overview of Xilinx's comprehensive development tools, go to the Developer Zone [Ref 21] on the Xilinx website. Xilinx's SoC and FPGA technology is becoming increasingly accessible to a wider range of engineers, including SW engineers and architects working at the system level. High levels of abstraction in the tools allow design entry using C/C++ [Ref 22] and at even higher levels of abstraction by using tools like MATLAB® and Simulink® from the Mathworks [Ref 23].

One of the key benefits of developing on a programmable platform is the ability to verify and validate the design including the RFFE on the same silicon that will be used in production. The co-verification of the DFE and RFFE can now be accomplished in a much more seamless and effortless way using a common design platform.

## Summary

Deploying next-generation radio solutions related to the RFFE has its challenges. Due to the combination of wider bandwidths and higher channel counts, it is clear that the interface between the DFE and RFFE must be eliminated. At the same time a wide range of radio types needs to be supported. A single flexible platform to reduce time to market and development costs is required.

A platform based on Xilinx's All Programmable SoCs and FPGAs with integrated RF-sampling data converters is a compelling solution that can satisfy these challenges. This disruptive technology is the closest solution yet to a true SDR implementation on a single device.

For more information, go to: [www.xilinx.com/RFSoc](http://www.xilinx.com/RFSoc).



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21. Xilinx website page: [Hardware Optimization](#)
22. Xilinx website page: [Vivado® High-Level Synthesis](#)
23. Xilinx website page: [System Generator](#)

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/27/2017	1.0.1	Typographical edits to <a href="#">Figure 2</a> .
02/17/2017	1.0	Initial Xilinx release.

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